TEXAS INSTRUMENTS
ADS127L11
SBAS946 – APRIL 2021

ADS127L11 400-kSPS, Wide-Bandwidth, 24-Bit, Delta-Sigma ADC

1 Features

- Programmable data rate:
  - Up to 400 kSPS (wideband filter)
  - Up to 1.067 MSPS (low-latency filter)
- Selectable digital filter:
  - Low-latency sinc filter
  - Wideband FIR filter
- AC and DC precision:
  - 111-dB dynamic range (200 kSPS)
  - –120-dB THD
  - 1-ppm of FS INL
  - 100-nV/°C offset drift
  - 0.5-ppm/°C gain drift
- Power-scalable ADC:
  - High-speed mode: 400 kSPS, 18.6 mW
  - Low-speed mode: 50 kSPS, 3.3 mW
- Input and reference precharge buffers
- Internal or external clock
- Unipolar or bipolar supply operation
- 3-mm × 3-mm, WQFN package option

2 Applications

- Test and measurement
  - Data acquisition (DAQ)
  - Shock and vibration instruments
  - Acoustics and dynamic strain gauges
- Factory automation and control
  - Condition monitoring
- Aerospace and defense
  - SONAR
- Medical
  - Electroencephalogram (EEG)
- Grid Infrastructure
  - Power quality analyzer

3 Description

The ADS127L11 is a 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) with data rates up to 400 kSPS using the wideband filter and up to 1067 kSPS using the low-latency filter. The device offers an excellent combination of ac performance and dc precision with low power consumption (18.6 mW in high-speed mode).

The device integrates input and reference precharge buffers to accept a variety of input amplifiers. The low drift modulator achieves excellent dc precision with low in-band noise for outstanding ac performance. The power-scalable architecture provides two speed modes to optimize data rate, resolution, and power consumption.

The digital filter is configurable to wideband or low-latency modes, allowing the user to optimize the filter for wideband ac performance or for data throughput, all in one device.

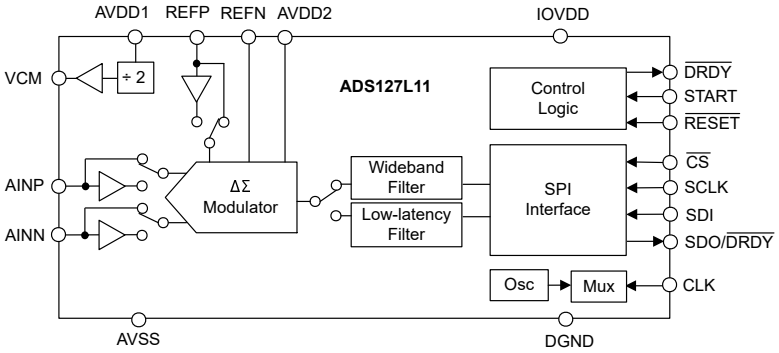
The serial interface features daisy-chain capability to simplify the SPI I/O over an isolation barrier. Input and output data are validated by cyclic-redundancy check (CRC) to enhance communication reliability.

The small 3-mm x 3-mm WQFN and 6.5-mm x 4.4-mm TSSOP packages are suitable for space-saving applications. The device is fully specified for operation over the –40°C to +125°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS127L11	WQFN (20)	3.00 mm × 3.00 mm
	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2021	*	Initial release.

5 Pin Configuration and Functions

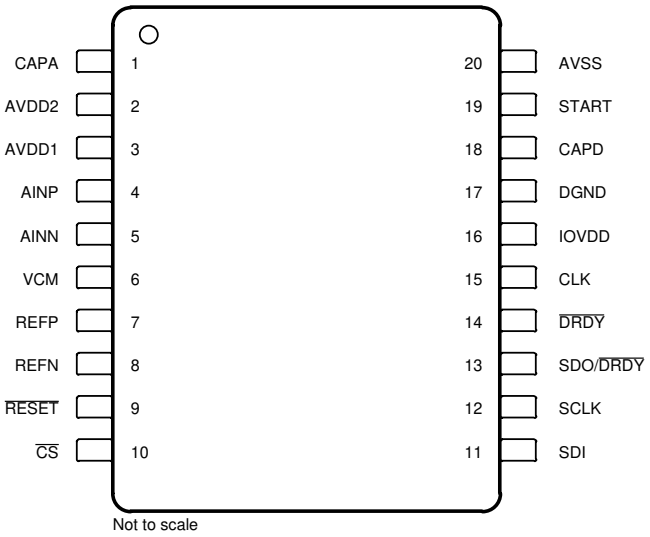

Figure 5-1. PW Package, 20-Pin TSSOP, Top View

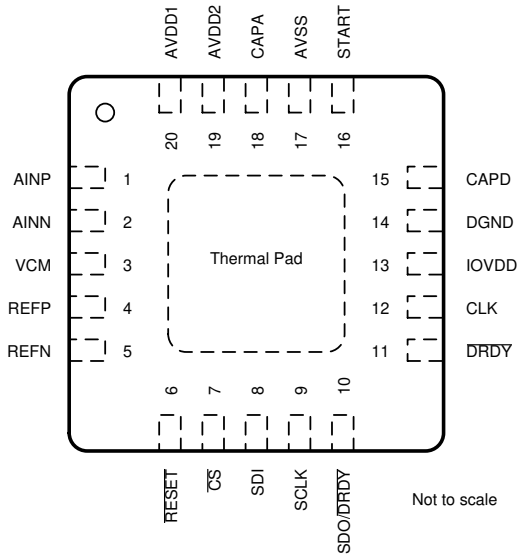

Figure 5-2. RUK Package, 20-Pin WQFN, Top View

Table 5-1. Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	TSSOP	WQFN		
AINN	5	2	Analog input	Negative analog input; see the Analog Input section for details
AINP	4	1	Analog input	Positive analog input; see the Analog Input section for details
AVDD1	3	20	Analog Supply	Positive analog supply 1; see the Power Supplies section for details
AVDD2	2	19	Analog Supply	Positive analog supply 2; see the Power Supplies section for details
AVSS	20	17	Analog Supply	Negative analog supply; see the Power Supplies section for details
CAPA	1	18	Analog output	Analog voltage regulator output capacitor bypass
CAPD	18	15	Analog output	Digital voltage regulator output capacitor bypass
CLK	15	12	Digital input	Clock input; see the ADC Clock section for details
$\overline{CS}$	10	7	Digital input	Chip select; active low; see the $\overline{CS}$ section for details
DGND	17	14	Ground	Digital ground
$\overline{DRDY}$	14	11	Digital output	Data ready; active low; see the Data Ready section for details
IOVDD	16	13	Digital Supply	I/O supply voltage; see the Power Supplies section for details
REFN	8	5	Analog input	Negative reference input; see the Reference Voltage section for details
REFP	7	4	Analog input	Positive reference input; see the Reference Voltage section for details
$\overline{RESET}$	9	6	Digital input	Reset; active low; see the Reset section for details
SCLK	12	9	Digital input	Serial data clock; see the SCLK section for details
SDI	11	8	Digital input	Serial data input; see the SDI section for details
SDO/$\overline{DRDY}$	13	10	Digital output	Serial data output and (optional) data ready; see the SDO/$\overline{DRDY}$ section for details
START	19	16	Digital input	Conversion start; see the Conversion Control section for details
VCM	6	3	Analog output	Common-mode voltage buffered output; see the VCM section for details
Thermal Pad	—	Pad	—	Thermal power pad; connect to AVSS.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Power supply voltage	AVDD1 to AVSS	–0.3	6.5	V
	AVDD2 to AVSS	–0.3	6.5	
	AVSS to DGND	–3	0.3	
	IOVDD to DGND	–0.3	6.5	
	IOVDD to AVSS		8.5	
Analog input voltage	AINP, AINN, REFP, REFN	AVSS – 0.3	AVDD1 + 0.3	V
Analog output voltage	CAPA	AVSS	1.65	V
	CAPD	DGND	1.65	
	VCM	AVSS	AVDD1	
Digital input/output voltage	$\overline{CS}$, SCLK, SDI, SDO/$\overline{DRDY}$, $\overline{DRDY}$, START, $\overline{RESET}$, CLK	DGND – 0.3	IOVDD + 0.3	V
Input current	Continuous, any pin except power-supply pins(2)	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Input and output pins are diode-clamped to the internal power supplies. Limit the input current to 10 mA in the event the analog input voltage exceeds AVDD1 + 0.3 V or AVSS – 0.3 V, or if the digital input voltage exceeds IOVDD + 0.3 V or DGND – 0.3 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVDD1 to AVSS, high-speed mode	4.5		5.5	V
		AVDD1 to AVSS, low-speed mode	2.85		5.5	
		AVDD1 to DGND	1.5			
		Absolute (AVSS / AVDD1) ratio			1.2	V/V
		AVDD2 to AVSS	1.74		5.5	V
		AVSS to DGND	–2.75		0	
	Digital power supply	IOVDD to DGND	1.65		5.5	V
ANALOG INPUTS						
V_{AINP}, V_{AINN}	Absolute input voltage	Precharge buffer off	AVSS – 0.05		AVDD1 + 0.05	V
		Precharge buffer on	AVSS + 0.1		AVDD1	
V_{IN}	Differential input voltage $V_{IN} = V_{AINP} – V_{AINN}$	1x input range	$–V_{REF}$		V_{REF}	V
		1x input range, extended mode	$–1.25·V_{REF}$		$1.25·V_{REF}$	
		2x input range	$–2·V_{REF}$		$2·V_{REF}$	
		2x input range, extended mode	$–2.5·V_{REF}$		$2.5·V_{REF}$	
VOLTAGE REFERENCE INPUTS						
V_{REF}	Differential Reference Voltage $V_{REF} = V_{REFP} – V_{REFN}$	Low reference range	0.5	2.5	2.75	V
		High reference range	1	4.096	AVDD1 – AVSS	
V_{REFN}	Negative reference voltage		AVSS – 0.05			V
V_{REFP}	Positive reference voltage	REFP precharge buffer off			AVDD1 + 0.05	V
		REFP precharge buffer on			AVDD1 – 0.7	
EXTERNAL CLOCK SOURCE						
f_{CLK}	Clock frequency	High-speed mode	0.5	25.6	26.2	MHz
		Low-speed mode	0.5	3.2	3.28	
DIGITAL INPUTS						
V_{IL}	Logic input voltage, low		DGND		0.3·IOVDD	V
V_{IH}	Logic input voltage, high		0.7·IOVDD		IOVDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–45		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		ADS127L11		UNIT
		WQFN (RUK)	TSSOP (PW)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.0	92.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.9	32.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.9	44.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.9	43.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.1	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

Minimum and maximum specifications apply from T_A = –40°C to +125°C; Typical specifications are at T_A = 25°C. All specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, 1x input range, f_{CLK} = 25.6 MHz (high-speed mode), f_{CLK} = 3.2 MHz (low-speed mode), input and reference precharge buffers on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS, HIGH-SPEED MODE						
	Input current, differential input voltage	Precharge buffers off		95		µA/V
		Precharge buffers off, 2x input range		45		
		Precharge buffers on		±3		µA
	Input current drift, differential input voltage	Precharge buffers off		2		nA/V/°C
		Precharge buffers off, 2x input range		1		
		Precharge buffers on		5		nA/°C
	Input current, common-mode input voltage	Precharge buffers off		4.5		µA/V
		Precharge buffers off, 2x input range		2.4		
		Precharge buffers on		±3		µA
ANALOG INPUTS, LOW-SPEED MODE						
	Input current, differential input voltage	Precharge buffers off		12		µA/V
		Precharge buffers off, 2x input range		6		
		Precharge buffers on		±0.4		µA
	Input current drift, differential input voltage	Precharge buffers off		2		nA/V/°C
		Precharge buffers off, 2x input range		1		
		Precharge buffers on		0.2		nA/°C
	Input current, common-mode input voltage	Precharge buffers off		0.6		uA/V
		Precharge buffers off, 2x input range		0.3		
		Precharge buffers on		±3		uA
DC PERFORMANCE						
	Resolution		24			Bits
	Noise		See Noise Performance for details			
f_{DATA}	Output data rate	High-speed mode, low-latency filter	0.08		1067	kSPS
		High-speed mode, wideband filter	3.125		400	
		Low-speed mode, low-latency filter	0.01		133	
		Low-speed mode, wideband filter	0.390625		50	
INL	Integral nonlinearity	Best-fit method		1	TBD	ppm of FSR
	Offset error	T_A = 25°C	–TBD	±30	TBD	µV
	Offset drift			100	TBD	nV/°C
	Gain error	T_A = 25°C	–TBD	±500	TBD	ppm of FSR
	Gain drift			0.5	TBD	ppm of FSR/°C
NMRR	Normal-mode rejection ratio	f_{IN} = 50 Hz (±1 Hz), f_{DATA} = 50 SPS	100			dB
		f_{IN} = 60 Hz (±1 Hz), f_{DATA} = 60 SPS	100			
CMRR	Common-mode rejection ratio	dc	TBD	120		dB
		dc to 10 kHz		120		
		dc, 2x input range		100		
PSRR	Power-supply rejection ratio	AVDD1, dc		90		dB
		AVDD2, dc		100		
		IOVDD, dc		100		

6.5 Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C; Typical specifications are at T_A = 25°C. All specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, 1x input range, f_{CLK} = 25.6 MHz (high-speed mode), f_{CLK} = 3.2 MHz (low-speed mode), input and reference precharge buffers on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE, HIGH-SPEED MODE						
DR	Dynamic range	Inputs shorted, OSR = 64, f_{DATA} = 200 kSPS				
		Wideband filter	TBD	111		dB
		Wideband filter, V_{REF} = 2.5 V		107		
		Wideband filter, V_{REF} = 2.5 V, 2x input range		108		
		Low-latency filter	TBD	114		
		Low-latency filter, V_{REF} = 2.5 V		110		
		Low-latency filter, V_{REF} = 2.5 V, 2x input range		111		
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, V_{IN} = –0.5 dBFS, OSR = 64, f_{DATA} = 200 kSPS				
		Wideband filter	TBD	110		dB
		Wideband filter, V_{REF} = 2.5 V		106		
		Wideband filter, V_{REF} = 2.5 V, 2x input range		107		
		Low-latency filter	TBD	113		
		Low-latency filter, V_{REF} = 2.5 V		109		
		Low-latency filter, V_{REF} = 2.5 V, 2x input range		110		
THD	Total harmonic distortion	f_{IN} = 1 kHz, V_{IN} = –0.5 dBFS, OSR = 64, f_{DATA} = 200 kSPS, 9 harmonics				
		Wideband filter		–120	TBD	dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz, V_{IN} = –0.5 dBFS, OSR = 64		125		dB
AC PERFORMANCE, LOW-SPEED MODE						
DR	Dynamic range	Inputs shorted, OSR = 64, f_{data} = 25 kSPS				
		Wideband filter	TBD	111		dB
		Wideband filter, V_{REF} = 2.5 V		107		
		Wideband filter, V_{REF} = 2.5 V, 2xinput range		108		
		Low-latency filter	TBD	114		
		Low-latency filter, V_{REF} = 2.5 V		110		
		Low-latency filter, V_{REF} = 2.5 V, 2x input range		111		
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, V_{IN} = –0.5 dBFS, OSR = 64, f_{data} = 25 kSPS				
		Wideband filter	TBD	110		dB
		Wideband filter, V_{REF} = 2.5 V		106		dB
		Wideband filter, V_{REF} = 2.5 V, 2x input range		107		dB
		Low-latency filter,	TBD	113		dB
		Low-latency filter, V_{REF} = 2.5 V		109		dB
		Low-latency filter, V_{REF} = 2.5 V, 2x input range		110		dB
THD	Total harmonic distortion	f_{IN} = 1 kHz, V_{IN} = –0.5 dBFS, OSR = 64, f_{data} = 25 kSPS, 9 harmonics				
		Wideband filter		–120	TBD	dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz, V_{IN} = –0.5 dBFS, OSR = 64		125		dB
WIDEBAND FILTER CHARACTERISTICS						
	Passband frequency	Within envelope of passband ripple		0.4·f_{DATA}		Hz
		–0.1-dB frequency		0.4125·f_{DATA}		
		–3-dB frequency		0.4374·f_{DATA}		
	Passband ripple		–0.0004		0.0004	dB
	Stopband frequency	At stopband attenuation		0.5·f_{DATA}		Hz
	Stopband attenuation			106		dB
	Group delay			34/f_{DATA}		s
	Settling time			68/f_{DATA}		s

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6.5 Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C; Typical specifications are at T_A = 25°C. All specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, 1x input range, f_{CLK} = 25.6 MHz (high-speed mode), f_{CLK} = 3.2 MHz (low-speed mode), input and reference precharge buffers on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE INPUTS						
	Input current, differential reference voltage	REFP precharge buffer off, high-speed mode		190		µA/V
		REFP precharge buffer off, low-speed mode		80		
		REFP only, precharge buffer on		±2		µA
	Input current drift	REFP precharge buffer off, high-speed mode		35		nA/°C
		REFP precharge buffer off, low-speed mode		12		
		REFP only, precharge buffer on		20		
INTERNAL OSCILLATOR						
	Frequency	High-speed mode	25.2	25.6	26	MHz
		Low-speed mode	3.15	3.2	3.25	
VCM OUTPUT VOLTAGE						
	Output voltage			(AVDD1 + AVSS) / 2		V
	Accuracy			±0.2%		
	Voltage noise	1-kHz bandwidth		25		$µV_{RMS}$
	Capacitive load				100	nF
	Resistive load		10			kΩ
	Short-circuit current limit			10		mA
DIGITAL INPUTS/OUTPUTS						
V_{OL}	Logic-low output level	OUT_DRV = 0b, I_{OL} = 2 mA			0.2·IOVDD	V
		OUT_DRV = 1b, I_{OL} = 1 mA			0.2·IOVDD	
V_{OH}	Logic-high output level	OUT_DRV = 0b, I_{OH} = –2 mA	0.8·IOVDD			V
		OUT_DRV = 1b, I_{OH} = –1 mA	0.8·IOVDD			
	Input hysteresis			70		mV
	Input current	Excluding $\overline{\text{RESET}}$ pin	–1		1	µA
	$\overline{\text{RESET}}$ pin pull-up resistor			20		kΩ
ANALOG SUPPLY CURRENT						
I_{AVDD1}, I_{AVSS}	AVDD1/AVSS current (All buffers off)	High-speed mode		1.7	TBD	mA
		Low-speed mode		0.25	TBD	
		Standby mode		35		µA
		Power-down mode		1		
	AVDD1/AVSS current (per buffer function)	AINx precharge buffer, high-speed mode		1.35	TBD	mA
		AINx precharge buffer, low-speed mode		0.2	TBD	
		REFP precharge buffer, high-speed mode		1.5	TBD	
		REFP precharge buffer, low-speed mode		0.4	TBD	
		VCM buffer		0.1		
I_{AVDD2}, I_{AVSS}	AVDD2/AVSS current	High-speed mode		3.5	TBD	mA
		Low-speed mode		0.85	TBD	
		Standby mode		55		µA
		Power-down mode		0.5		

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6.5 Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C; Typical specifications are at T_A = 25°C. All specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, 1x input range, f_{CLK} = 25.6 MHz (high-speed mode), f_{CLK} = 3.2 MHz (low-speed mode), input and reference precharge buffers on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL SUPPLY CURRENT						
I_{IOVDD}	IOVDD current	High-speed mode, wideband filter		2.1	TBD	mA
		High-speed mode, low-latency filter		0.8	TBD	
		Low-speed mode, wideband filter		0.3	TBD	
		Low-speed mode, low-latency filter		0.15	TBD	
		Standby mode, external clock		10		µA
		Standby mode, internal oscillator		40		
		Power-down mode		10		
POWER DISSIPATION						
P_D	Power dissipation	AVDD1 = 5 V, AVSS = 0 V, AVDD2 = 1.8 V, IOVDD = 1.8 V, precharge buffers off				
		High-speed mode, wideband filter		18.6		mW
		High-speed mode, low-latency filter		16.2		
		Low-speed mode, wideband filter		3.3		
		Low-speed mode, low-latency filter		3.1		

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6.6 Timing Requirements (1.65 V ≤ IOVDD ≤ 2 V)

over operating ambient temperature range, unless otherwise noted

		MIN	MAX	UNIT
CLK PIN				
$t_{c(CLK)}$	CLK period, high-speed mode	38	2000	ns
	CLK period, low-speed mode, CLK_DIV = 1b	38	2000	
	CLK period, low-speed mode, CLK_DIV = 0b	305	2000	
$t_{w(CLKL)}$	Pulse duration, CLK low	17		ns
$t_{w(CLKL)}$	Pulse duration, CLK low, low-speed mode, CLK_DIV = 0b	128		ns
$t_{w(CLKH)}$	Pulse duration, CLK high	17		ns
$t_{w(CLKH)}$	Pulse duration, CLK high, low-speed mode, CLK_DIV = 0b	128		ns
SERIAL INTERFACE				
$t_{c(SC)}$	SCLK period	25	$1/(4 \cdot f_{DATA})$	ns
$t_{w(SCL)}$	Pulse duration, SCLK low	10		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	10		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	10		ns
$t_{su(DI)}$	Setup time, SDI valid before SCLK falling edge	4		ns
$t_{h(DI)}$	Hold time, SDI valid after SCLK falling edge	6		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	20		ns
RESET PIN				
$t_{w(RSL)}$	Pulse duration, $\overline{RESET}$ low	4		t_{CLK}
$t_{d(RSSC)}$	Delay time, communication start after $\overline{RESET}$ rising edge or after SPI RESET pattern	10000		t_{CLK}
START PIN				
$t_{w(STL)}$	Pulse duration, START low	4		t_{CLK}
$t_{w(STH)}$	Pulse duration, START high	4		t_{CLK}
$t_{su(STCLK)}$	Setup time, START high before CLK rising edge (1)	9		ns
$t_{h(STCLK)}$	Hold time, START high after CLK rising edge (1)	9		ns
$t_{su(STDR)}$	Setup time, START falling edge or STOP bit before $\overline{DRDY}$ falling edge to stop next conversion (start/stop conversion mode)	8		t_{CLK}

(1) START rising edge should not be applied between the setup and hold time period at the rising edge of CLK

6.7 Switching Characteristics (1.65 V ≤ IOVDD ≤ 2 V)

over operating ambient temperature range, OUT_DRV = 0b, C_{LOAD} = 20 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to SDO/$\overline{DRDY}$ driven state				20	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to SDO/$\overline{DRDY}$ high impedance state				20	ns
$t_{h(SCDO)}$	Hold time, SCLK rising edge to invalid SDO/$\overline{DRDY}$		3			ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid SDO/$\overline{DRDY}$				23	ns
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high		2			t_{CLK}
$t_{p(SCDR)}$	Propagation delay time, 8th SCLK falling edge to $\overline{DRDY}$ return high	Synchronized and Start/stop modes			4	t_{CLK}
$t_{p(DRDO)}$	Propagation delay time, first SCLK rising edge of read operation for SDO/$\overline{DRDY}$ transition from $\overline{DRDY}$ mode to valid SDO	SDO_DRDY = 1b	30			ns
$t_{p(DODR)}$	Propagation delay time, last SCLK falling edge of read operation for SDO/$\overline{DRDY}$ transition from SDO to $\overline{DRDY}$ mode	SDO_DRDY = 1b	30			ns

6.8 Timing Requirements (2 V < IOVDD ≤ 5.5 V)

over operating ambient temperature range, unless otherwise noted

		MIN	MAX	UNIT
CLK PIN				
$t_{c(CLK)}$	CLK period, high-speed mode	38	2000	ns
	CLK period, low-speed mode, CLK_DIV = 1b	38	2000	
	CLK period, low-speed mode, CLK_DIV = 0b	305	2000	
$t_{w(CLKL)}$	Pulse duration, CLK low	17		ns
$t_{w(CLL)}$	Pulse duration, CLK low, low-speed mode	128		ns
$t_{w(CLKH)}$	Pulse duration, CLK high	17		ns
$t_{w(CLH)}$	Pulse duration, CLK high, low-speed mode	128		ns
SERIAL INTERFACE				
$t_{c(SC)}$	SCLK period	20	$1/(4 \cdot f_{DATA})$	ns
$t_{w(SCL)}$	Pulse duration, SCLK low	8		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	8		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	10		ns
$t_{su(DI)}$	Setup time, SDI valid before SCLK falling edge	4		ns
$t_{h(DI)}$	Hold time, SDI valid after SCLK falling edge	6		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	20		ns
RESET PIN				
$t_{w(RSL)}$	Pulse duration, $\overline{RESET}$ low	4		t
$t_{d(RSSC)}$	Delay time, first SCLK rising edge after $\overline{RESET}$ rising edge or SPI reset	10000		t_{CLK}
START PIN				
$t_{w(STL)}$	Pulse duration, START low	4		t_{CLK}
$t_{w(STH)}$	Pulse duration, START high	4		t_{CLK}
$t_{su(STCLK)}$	Setup time, START valid before CLKIN rising edge (1)	9		ns
$t_{h(STCLK)}$	Hold time, START valid after CLKIN rising edge (1)	9		ns
$t_{su(STDR)}$	Setup time, START falling edge or STOP bit before $\overline{DRDY}$ falling edge to stop next conversion (start/stop conversion mode)	8		t_{CLK}

(1) START rising edge should not be applied between the setup and hold time period at the rising edge of CLKIN

6.9 Switching Characteristics (2 V < IOVDD ≤ 5.5 V)

over operating ambient temperature range, OUT_DRV = 0b, C_{LOAD} = 20 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to SDO/$\overline{DRDY}$ driven				17	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to SDO/$\overline{DRDY}$ high impedance				17	ns
$t_{h(SCDO)}$	Hold time, SCLK rising edge to invalid SDO/$\overline{DRDY}$		3			ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid new SDO/$\overline{DRDY}$				19	ns
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high		2			t_{CLK}
$t_{p(SCDR)}$	Propagation delay time, 8th SCLK falling edge to $\overline{DRDY}$ high	Synchronized and Start/stop modes			4	t_{CLK}
$t_{p(DRDO)}$	Propagation delay time, first SCLK rising edge of read operation for SDO/$\overline{DRDY}$ transition from $\overline{DRDY}$ mode to valid SDO	SDO_DRDY = 1b	20			ns
$t_{p(DODR)}$	Propagation delay time, last SCLK falling edge of read operation for SDO/$\overline{DRDY}$ transition from SDO to $\overline{DRDY}$ mode	SDO_DRDY = 1b	20			ns

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6.10 Timing Diagrams

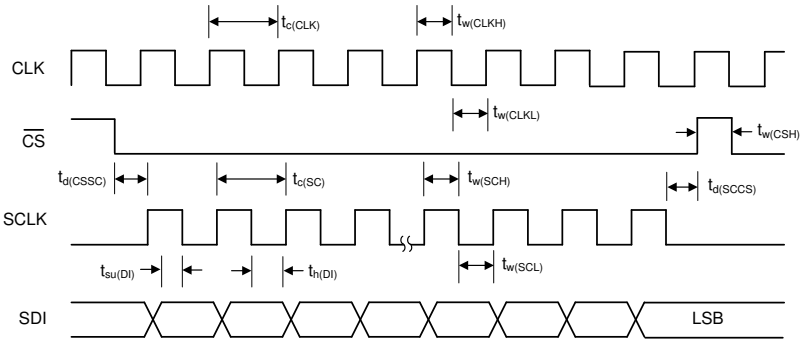


Figure 6-1. Clock and Serial Interface Timing Requirements

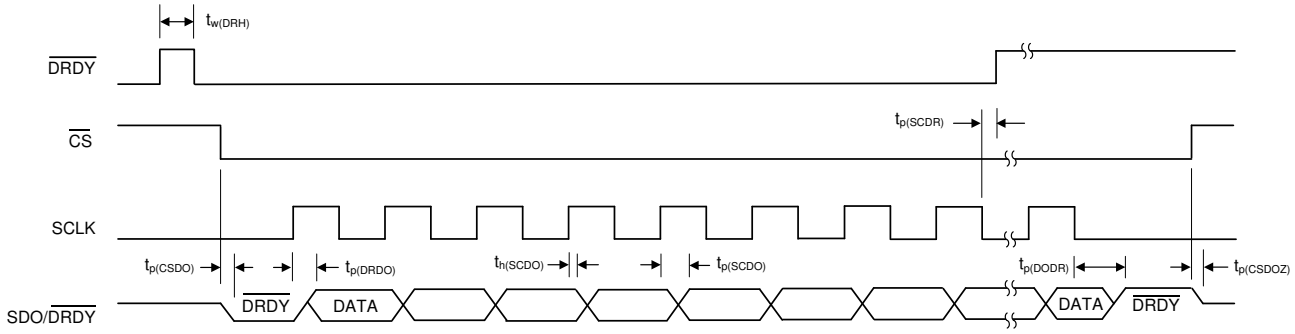


Figure 6-2. Serial Interface Switching Characteristics

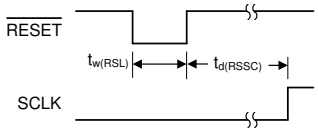


Figure 6-3. $\overline{RESET}$ Pin Timing

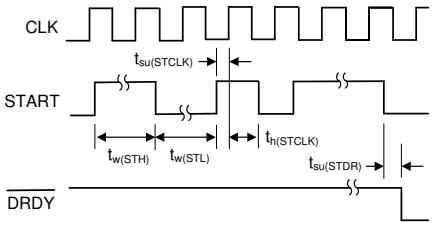


Figure 6-4. START Pin Timing

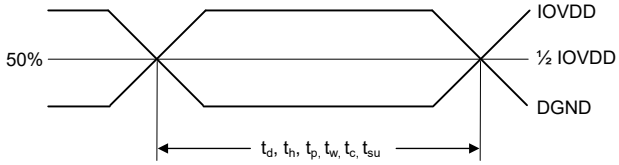
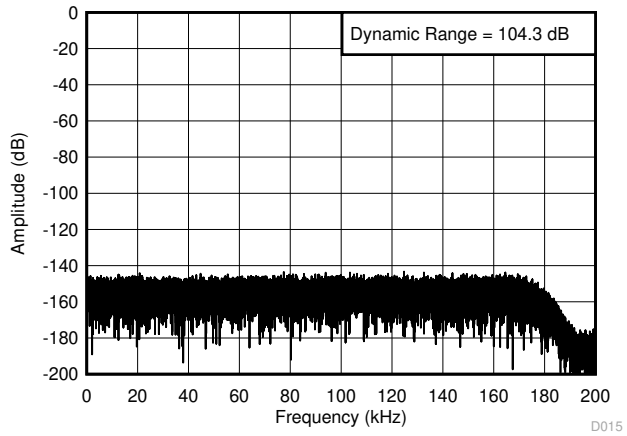


Figure 6-5. Timing Reference

6.11 Typical Characteristics

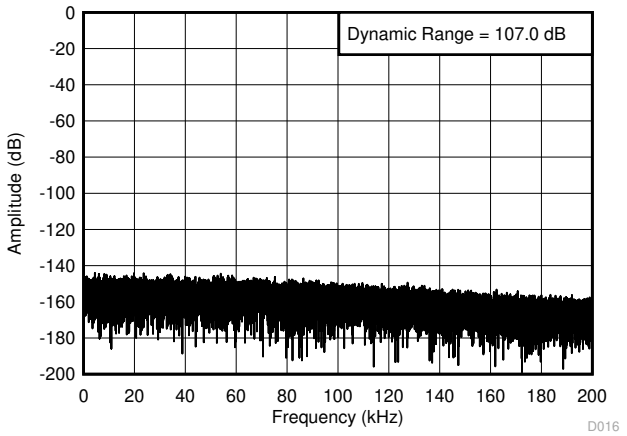
AVDD1 = 5 V, AVDD2 = 5 V, IOVDD = 1.8 V, V_{REF} = 2.5 V, input and reference precharge buffers on, T_A = 25°C (unless otherwise noted)



Inputs shorted, wideband filter, 400 kSPS, 400k samples

V_{REF} = 2.5 V

Figure 6-6. Output Spectrum



Inputs shorted, sinc4 filter, 400 kSPS, 400k samples

V_{REF} = 2.5 V

Figure 6-7. Output Spectrum

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7 Parameter Measurement Information

7.1 Noise Performance

The ADC provides two operational speed modes (high speed and low speed) allowing the user the trade-off of resolution, power consumption, and signal bandwidth. The low-speed mode operates the modulator at 1/8th speed, as a result the output data rates are reduced 1/8th to decrease the device power consumption. The programmable over-sampling ratio (OSR) determines the output data rate and associated signal bandwidth, therefore determining total noise performance. Increasing the OSR lowers the signal bandwidth and total noise by averaging more samples from the modulator to yield one conversion result.

The wideband filter provides data rates up to 400 kSPS in high-speed mode and 50 kSPS in low-speed mode. The low-latency sinc4 filter provides data rates up to 1.067 MSPS in high-speed mode and up to 133 kSPS in low-speed mode. The low-latency filter provides the options of sinc4, sinc4 + sinc1, sinc3, and sinc3 + sinc1 configurations.

Table 7-1 through Table 7-5 summarize the noise performance and signal bandwidth of the filters. Noise performance is shown with 1x input range and a 4.096-V reference voltage. Operating the device using a 2.5-V reference voltage decreases dynamic range by 4 dB (typical). The 2x input range option (only available for 2.5-V reference voltage) increases dynamic range by 1 dB (typical).

Noise data are representative of typical performance at T_A = 25°C and are the result of the standard deviation (rms) of the conversion data with inputs shorted and biased to mid-supply. A minimum of 1,000 consecutive conversions are used to calculate the total RMS noise (e_n). Because of the statistical nature of noise, repeated noise measurements may yield higher or lower noise results.

Equation 1 converts total RMS noise to dynamic range (dB) and Equation 2 converts total RMS noise to effective resolution (bits).

$$\text{Dynamic Range (dB)} = 20 \cdot \log(\text{FSR}/(2 \cdot \sqrt{2} \cdot e_n)) \quad (1)$$

$$\text{Effective Resolution (bits)} = 3.32 \cdot \log(\text{FSR}/e_n) \quad (2)$$

where FSR = $2 \cdot V_{REF}$ (1x input range), FSR = $4 \cdot V_{REF}$ (2x input range)

Table 7-1. Wideband Filter Performance (V_{REF} = 4.096 V, 1x input range)

OSR	DATA RATE (kSPS)	–0.1-dB FREQUENCY (kHz)	NOISE (e_n) (μV_{RMS})	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)					
32	400	165.000	10.6	108.7	19.5
64	200	82.500	7.47	111.8	20.1
128	100	41.250	5.20	114.9	20.6
256	50	20.625	3.66	118.0	21.1
512	25	10.312	2.58	121.0	21.6
1024	12.5	5.156	1.83	124.0	22.1
2048	6.25	2.578	1.29	127.0	22.6
4096	3.125	1.289	0.92	130.0	23.1
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)					
32	50	20.625	10.6	108.7	19.5
64	25	10.312	7.47	111.8	20.1
128	12.5	5.156	5.20	114.9	20.6
256	6.25	2.578	3.66	118.0	21.1
512	3.125	1.289	2.58	121.0	21.6
1024	1.5625	0.645	1.83	124.0	22.1
2048	0.78125	0.322	1.29	127.0	22.6
4096	0.390625	0.161	0.92	130.0	23.1

Table 7-2. Sinc4 Filter Performance (V_{REF} = 4.096 V, 1x input range)

OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)	NOISE (e_n) (μV_{RMS})	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)					
12	1066.666	242.666	76.3	91.6	16.7
16	800	182.000	27.3	100.5	18.2
24	533.333	121.333	10.4	108.9	19.6
32	400	91.000	7.96	111.2	20.0
64	200	45.500	5.57	114.3	20.5
128	100	22.750	3.90	117.4	21.0
256	50	11.375	2.80	120.3	21.5
512	25	5.687	1.98	123.3	22.0
1024	12.5	2.844	1.40	126.3	22.5
2048	6.25	1.422	0.99	129.3	23.0
4096	3.125	0.711	0.70	132.3	23.5
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)					
12	133.333	30.333	76.3	91.6	16.7
16	100	22.750	27.3	100.5	18.2
24	66.666	15.166	10.4	108.9	19.6
32	50	11.375	7.96	111.2	20.0
64	25	5.687	5.57	114.3	20.5
128	12.5	2.844	3.90	117.4	21.0
256	6.25	1.422	2.80	120.3	21.5
512	3.125	0.711	1.98	123.3	22.0
1024	1.5625	0.355	1.40	126.3	22.5
2048	0.78125	0.177	0.99	129.3	23.0
4096	0.390625	0.089	0.70	132.3	23.5

Table 7-3. Sinc4 + Sinc1 Filter Performance (V_{REF} = 4.096 V, 1x input range)

SINC4 OSR	SINC1 OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)	NOISE (e_n) (μV_{RMS})	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)						
32	2	200	68.35	5.63	114.2	20.5
32	4	100	40.97	3.98	117.2	21.0
32	10	40	17.47	2.81	120.3	21.5
32	20	20	8.814	1.99	123.3	22.0
32	40	10	4.420	1.41	126.3	22.5
32	100	4	1.770	0.99	129.3	23.0
32	200	2	0.885	0.70	132.3	23.5
32	400	1	0.442	0.52	134.9	23.9
32	1000	0.4	0.177	0.39	137.4	24.3
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)						
32	2	25	8.544	5.63	114.2	20.5
32	4	12.5	5.121	3.98	117.2	21.0
32	10	5	2.184	2.81	120.3	21.5
32	20	2.5	1.102	1.99	123.3	22.0
32	40	1.25	0.552	1.41	126.3	22.5
32	100	0.5	0.221	0.99	129.3	23.0
32	200	0.25	0.111	0.70	132.3	23.5
32	400	0.125	0.055	0.52	134.9	23.9
32	1000	0.05	0.022	0.39	137.4	24.3

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Table 7-4. Sinc3 Filter Performance (V_{REF} = 4.096 V, 1x input range)

OSR	DATA RATE (SPS)	–3-dB FREQUENCY (Hz)	NOISE (e_n) (μV_{RMS}) (1)	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)					
26667	480	126	0.29	140.0	24.7
32000	400	105	0.27	140.6	24.8
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)					
26667	60	16	0.29	140.0	24.7
32000	50	13	0.27	140.6	24.8

(1) The measurement of noise may vary due to the effects of 24-bit quantization: 4.096 V/2^{23} = 0.488 µV/code

Table 7-5. Sinc3 + Sinc1 Filter Performance (V_{REF} = 4.096 V, 1x input range)

SINC3 OSR	SINC1 OSR	DATA RATE (SPS)	–3-dB FREQUENCY (Hz)	NOISE (e_n) (μV_{RMS}) (1)	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)						
32000	3	133.3	54	0.19	143.7	25.3
32000	5	80	34	0.15	145.7	25.7
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)						
32000	3	16.6	6.7	0.19	143.7	25.3
32000	5	10	4.3	0.15	145.7	25.7

(1) The measurement of noise may vary due to the effects of 24-bit quantization: 4.096 V/2^{23} = 0.488 µV/code

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8 Detailed Description

8.1 Overview

The ADS127L11 is a high performance, 24-bit delta-sigma (ΔΣ) ADC offering a combination of excellent dc accuracy and ac precision. The device is optimized to provide very high resolution with low power consumption. Integrated input and reference precharge buffers relax the need of high bandwidth input drivers. The digital filter consists of two programmable modes: low-latency mode for dc applications and wideband mode for ac applications.

The ADC employs a delta-sigma modulator that measures the input voltage using the reference voltage to yield a one's-density bitstream that, in turn, is proportional to the input signal. The integrator stages of the modulator shift the quantization noise to an out-of-band frequency range where it is removed by the digital filter. The noise remaining within the pass band is thermal noise, which is reduced by the amount of oversampling programmed in the digital filter. The oversampling operation of the digital filter averages noise while also decimating the modulator data to yield the final output data.

The *Functional Block Diagram* shows the features of the ADS127L11. The ADC is a sampled-input, third-order delta-sigma modulator, that measures the differential input signal, $V_{IN} = (V_{AINP} – V_{AINN})$, against the differential reference, $V_{REF} = (V_{REFP} – V_{REFN})$. Input and positive reference precharge buffers greatly reduce the bandwidth requirement of the external input driver. The VCM output provides a mid-supply output voltage to drive the common-mode input of full differential amplifiers.

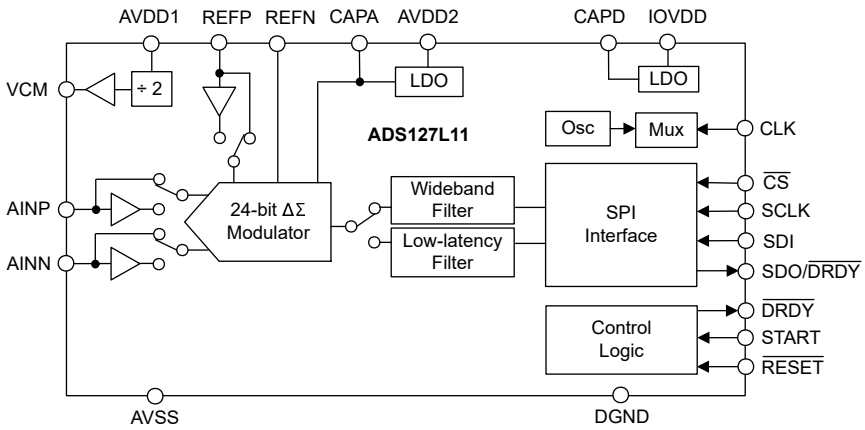
The two digital filter modes offer the choice of low-latency response or flat pass-band performance. The low-latency filter is programmable to sinc4, sinc4 + sinc1, sinc3 and sinc3 + sinc1 modes, allowing the user to optimize between noise performance and latency. The sinc3 + sinc1 filter provides rejection at 400 Hz, 60 Hz, 50 Hz, and 16.6 Hz. The wideband filter is a multi-tap FIR design providing outstanding frequency response with low pass-band ripple, steep transition-band, and high stop-band attenuation. Programmable oversampling ratio (OSR) and two speed modes allows optimization between bandwidth, resolution and device power consumption.

The serial interface is SPI-compatible and is used for device configuration and to read conversion data. The interface features daisy-chain capability for convenient connection of multi-channel, simultaneous-sampled systems. Integrated CRC error detection improves system-level reliability. $\overline{DRDY}$ is the conversion data ready output signal.

The device can be operated by an external clock for ac or dc applications, or by the internal oscillator for dc applications. The START pin synchronizes the start of digital filter process. The $\overline{RESET}$ pin resets the ADC.

Supply voltage AVDD1 powers the precharge buffers and the input sampling switches. AVDD2 powers the modulator via an internal regulator (CAPA). Supply voltage IOVDD is the digital I/O voltage which also powers the digital core via an internal regulator (CAPD). The internal regulators minimize overall power consumption and enable consistent levels of performance.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Analog Input (AINP, AINN)

The analog input is differential, with the input defined as a difference voltage: $V_{IN} = V_{AINP} – V_{AINN}$. For best performance, drive the input with a differential signal, with the common-mode voltage centered to mid-supply (AVDD1 + AVSS) / 2.

The ADC can accept either unipolar or bipolar input signals by configuring AVDD1 and AVSS accordingly. Figure 8-1 shows an example of a differential signal with a unipolar supply configuration. The common-mode voltage of the signal is set to mid-supply (AVDD1/2). Set AVDD1 = 5 V and AVSS = 0 V in this case. The VCM pin provides a buffered common-mode supply voltage to drive the output common-mode voltage of external amplifiers.

Figure 8-2 shows an example of a differential signal applied with a bipolar supply configuration. The common-mode voltage of the signal set to DGND. Set AVDD1 and AVSS to ±2.5 V for this operation. For bipolar and unipolar power supply configurations, the ADC can also be driven by a single-ended signal, with the AINN input tied to ground or mid-supply. However, because the signal range of a single-ended signal is limited to ±2.5 V (5-V total), reference voltage operation is therefore limited to 2.5 V.

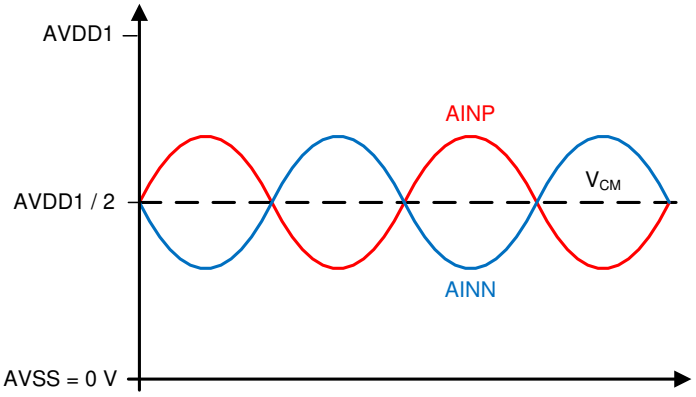

Figure 8-1. Unipolar Differential Input Signal

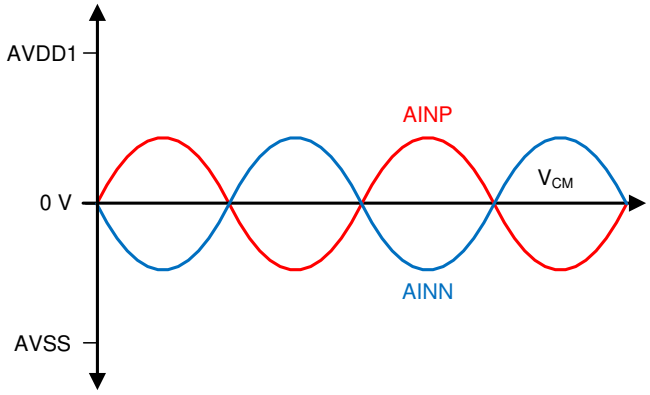

Figure 8-2. Bipolar Differential Input Signal

The analog inputs can be represented by the simplified circuit of Figure 8-3.

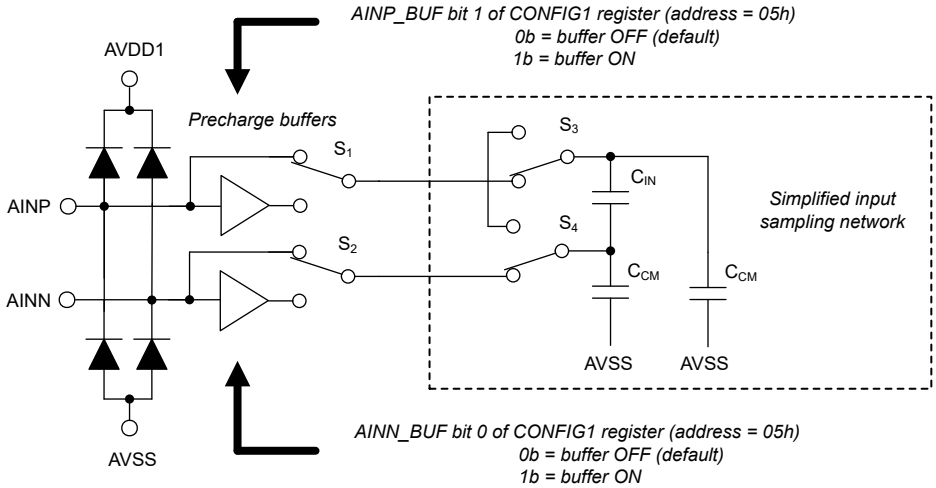

Figure 8-3. Analog Input Circuit

Diodes protect the ADC inputs from ESD events that occur during the manufacturing process and during PCB assembly when manufactured in an ESD-controlled environment. If the inputs are driven below AVSS – 0.3 V, or above AVDD1 + 0.3 V, the protection diodes may conduct. If these conditions are possible, use external clamp diodes, series resistors, or both to limit the input current to the specified value.

The device provides the option of using input precharge buffers. The buffers reduce the amplitude of the current required to charge the input sampling capacitor (C_{IN}). During the input sample phase, the buffers provide the coarse charge to C_{IN}. Approximately half-way through the sample phase, the precharge buffers are bypassed (S1 and S2 in up positions) resulting in the external driver providing the fine charge to C_{IN}. After completion of the sample phase, C_{IN} is discharged during the hold phase. The net effect of the buffers is to reduce the bandwidth requirement of the external driver that is needed to supply fully-settled, instantaneous input charge. The input buffers are enabled by the AINP_BUF and AINN_BUF bits of the CONFIG1 register.

When operating without the precharge buffers, the charge drawn by the input sampling capacitor can be modeled as an effective input impedance. The input current is comprised of differential and absolute components as shown in Equation 3 and Equation 4.

$$\text{Input Current, Differential Input Voltage} = f_{MOD} \cdot C_{IN} \cdot 10^6 \ (\mu A/V) \quad (3)$$

where

- $f_{MOD} = f_{CLK}/2$ = 12.8 MHz (high-speed mode), 1.6 MHz (low-speed mode)
- C_{IN} = 7.4 pF (1x input range), 3.6 pF (2x input range)

$$\text{Input Current, Absolute Input Voltage} = f_{MOD} \cdot C_{CM} \cdot 10^6 \ (\mu A/V) \quad (4)$$

where

- $f_{MOD} = f_{CLK}/2$ = 12.8 MHz (high-speed mode), 1.6 MHz (low-speed mode)
- C_{CM} = 0.35 pF (1x input range), 0.17 pF (2x input range)

For f_{MOD} = 12.8 MHz, C_{IN} = 7.4 pF and C_{CM} = 0.35 pF, the input current due to the differential voltage is 95 µA/V and the input current due to the absolute voltage is 4.5 µA/V. For example, if AINP = 4.5 V and AINN = 0.5 V, then V_{IN} = 4 V. The total AINP input current = (4 V·95 µA/V) + (4.5 V·4.5 µA/V) = 400 µA, and the total AINN current is (–4 V·95 µA/V) + (0.5 V·4.5 µA/V) = –378 µA.

The charge demand of the input sampling capacitor requires the input driver to settle within a half cycle of the modulator frequency $t = 1 / (2 \cdot f_{MOD})$. In order to satisfy this requirement, typically the driver bandwidth will be much larger than the one required by the signal. The bandwidth of the driver can be determined sufficient when THD and SNR data sheet performance are achieved. In the low-speed mode of operation, the modulator sampling is 8x slower, therefore allowing more time for the driver to settle.

8.3.1.1 Input Range

The ADC offers the option of two input voltage ranges: $V_{IN} = \pm V_{REF}$ and $V_{IN} = \pm 2 \cdot V_{REF}$. The 2x range doubles the differential input range to ±5 V when operating with a 2.5-V reference voltage. The 2x input range option improves SNR 1 dB (typical) compared to the 1x range using the same 2.5-V reference. However, SNR performance is typically improved 4 dB by increasing the reference voltage to 4.096 V or 5 V using the high-voltage reference range mode with the 1x input range. See the CONFIG1 register to program the input range.

The ADC also offers the option of extending the input signal range by 25%. This option allows the conversion of input signals exceeding the standard range of $\pm k \cdot V_{REF}$ up to the extended range of $\pm 1.25 \cdot k \cdot V_{REF}$, where k = 1 for 1x range option or k = 2 for 2x input range option. Output data is scaled such that the positive and negative full-scale output codes (7FFFFFh and 800000h) occur at $\pm 1.25 \cdot k \cdot V_{REF}$. Operating the input voltage in the extended range (from 100% to 125% FS) results in gradual increase of conversion noise. See the CONFIG2 register to program the extended range mode. Table 8-1 summarizes the ADC input range options. The maximum value of the reference voltage depends on the input range and the limitation of the analog power supply voltage. For example, with an input range of $\pm 2.5 \cdot V_{REF}$ and a 5-V power supply, the reference voltage is limited to 2 V in order to be able to use the full input range.

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Table 8-1. ADC Input Range Options

INP_RNG BIT	EXT_RNG BIT	INPUT RANGE (V)
0	0	$\pm V_{REF}$
1	0	$\pm 2 \cdot V_{REF}$
0	1	$\pm 1.25 \cdot V_{REF}$
1	1	$\pm 2.5 \cdot V_{REF}$

8.3.2 Reference Voltage (REFP, REFN)

A reference voltage is required for operation. The reference voltage input is differential, defined as: $V_{REF} = V_{REFP} - V_{REFN}$, applied to inputs REFP and REFN. See the Recommended Operating Conditions for the valid reference voltage range.

The reference inputs have an input structure similar to the analog inputs with the circuitry shown in Figure 8-4. ESD diodes protect the reference inputs. To keep these diodes from turning on, make sure the voltages on the reference pins do not go below AVSS by more than 0.3 V, or above AVDD1 by 0.3 V. If these conditions are possible, use external clamp diodes, series resistors, or both to limit the input current to the specified value.

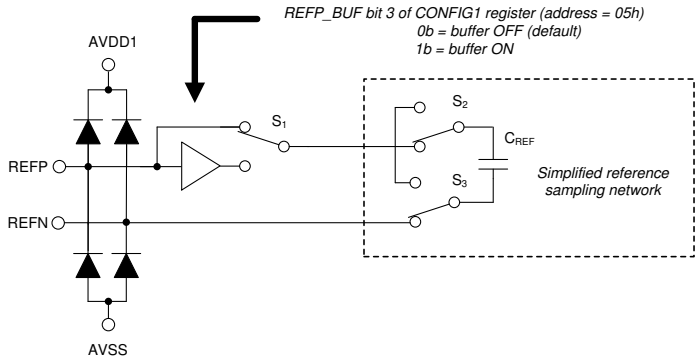

Figure 8-4. Reference Input Circuit

The reference voltage is sampled by a sampling capacitor C_{REF}. In unbuffered mode, current flows through the reference inputs to charge the sampling capacitor. The current consists of a dc component and an ac component that varies with the frequency of the modulator sampling clock. See the Electrical Characteristics for the reference input current specification.

The charge drawn by the reference sampling capacitor requires the external reference driver to settle at the end of the sample phase $t = 1 / (2 \cdot f_{MOD})$. Incomplete settling can result in degradation of THD, SNR and gain error. The bandwidth of the reference driver is satisfactory when data sheet performance is achieved. Operation in low-speed mode reduces the modulator sampling clock frequency by 1/8th, therefore allowing more time for the reference driver to settle.

The ADC integrates a precharge buffer for the REFP input to reduce the charge drawn by the sampling capacitor. The precharge buffer provides the coarse charge to the reference sampling capacitor C_{REF}. Approximately half-way through the sample phase, the precharge buffer is bypassed (S1 in up position), at which time the external driver provides the fine charge to the sampling capacitor.

Many applications either ground REFN, or connect REFN to AVSS. A precharge buffer for REFN is not necessary for these cases. For applications when REFN is not a low impedance source, consider buffering REFN.

8.3.2.1 Reference Voltage Range

Operation of the ADC is optimized by separating the reference voltage into two operating ranges: low range and high range. In general, the low range is used with reference voltage ≤ 2.5 V, and the high range is used with reference voltage > 2.5 V. If the high reference range is selected, the input range is forced to 1x.

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See the REF_RNG bit in the CONFIG1 register to program the appropriate reference voltage range. See the Recommended Operating Conditions for the valid reference voltage pertaining to each reference range.

8.3.3 ADC Clock

Figure 8-5 shows the block diagram of the clock input circuit. The ADC can be operated using internal oscillator, or external clock. External clock operation is by applying the clock to the CLK pin and setting the CLK_SEL bit = 1b of the CONFIG4 Register. The nominal values of f_{CLK} are 25.6 MHz in high-speed mode and 3.2 MHz in low-speed mode. A divide-by-eight option is available at the CLK input intended to divide a fast clock input for the low-speed mode of operation. f_{CLK} is internally divided by two to derive the modulator sampling clock (f_{MOD}).

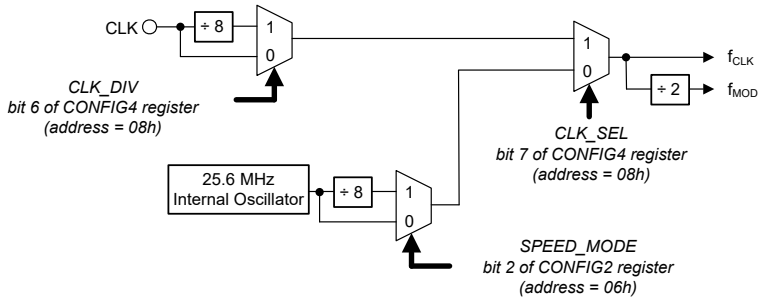

Figure 8-5. Clock Block Diagram

8.3.3.1 Internal Oscillator

At power-up and reset, the ADC defaults to internal oscillator operation (CLK_SEL bit = 0b). The frequency of the internal oscillator automatically scales for high-speed or low-speed modes. Because the clock jitter of the internal oscillator causes a reduction in SNR, the internal oscillator operation is not recommended for measurement of ac signals.

8.3.3.2 External Clock

To operate the ADC with an external clock, first apply the clock signal to the CLK pin and then program the CLK_SEL bit to 1b. A divide-by-eight clock option is available to operate the ADC in low-speed mode using a 25.6 MHz clock (CLK_DIV bit = 1b). The clock frequency can be decreased from the nominal value to produce any specific data rate between the standard values. However, because the OSR of the ADC does not change when the clock frequency is changed, the conversion noise of the new data rate remains the same.

When measuring ac signals, a low-jitter clock is essential for data sheet SNR performance. Uncertainty of the input sampling instant caused by clock jitter can degrade SNR performance. For example, for a 200-kHz f_{IN} input signal, an external clock with better than 10-ps (rms) jitter is required. For lower input frequencies, the clock jitter can be relaxed –20 dB per decade. For example, at f_{IN} = 20 kHz, clock jitter of 100-ps can be tolerated. A crystal-derived clock oscillator is the recommended clock source. Avoid ringing on the clock input. A series resistor placed at the output of the clock buffer often helps to reduce ringing.

8.3.4 Digital Filter

The digital filter performs low-pass filtering and decimation on the low-resolution, high-speed data from the modulator to produce the higher-resolution, lower-speed, final output data. The ADC offers the user the choice of two filter modes: wideband and low-latency. The selected filter mode optimizes either the frequency characteristics (wideband filter mode) or the time characteristics (low-latency filter mode).

8.3.4.1 Wideband Filter

The wideband filter is a multistage FIR topology featuring linear phase response, low passband ripple, narrow transition-band, and high stopband attenuation. The filter is well suited for measuring both ac and dc signals. Eight programmable oversampling ratios (OSR) and two speed modes yield 16 possible output data rates. The programmability of OSR and speed modes allow optimization of bandwidth, resolution, and device power consumption.

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Figure 8-6 through Figure 8-9 show the frequency response of the wideband filter. Figure 8-6 shows the frequency response to f_{DATA}. The stopband is in full effect at $f_{DATA}/2$ to prevent aliasing at the Nyquist frequency. Figure 8-7 shows the passband ripple. Figure 8-8 shows the detailed frequency response at the transition band. Figure 8-9 shows the filter response repeating at f_{MOD}. If the input signal frequency at f_{MOD} is not attenuated by an analog anti-aliasing filter, frequency aliasing will occur at discrete frequency intervals beginning at the first multiple of f_{MOD}. These frequency intervals are defined by: $(N \cdot f_{MOD}) \pm f_{BW}$, where *N* are the multiples of f_{MOD}: 1, 2, 3 and so on, f_{MOD} is the modulator sampling frequency and f_{BW} is the bandwidth of the filter.

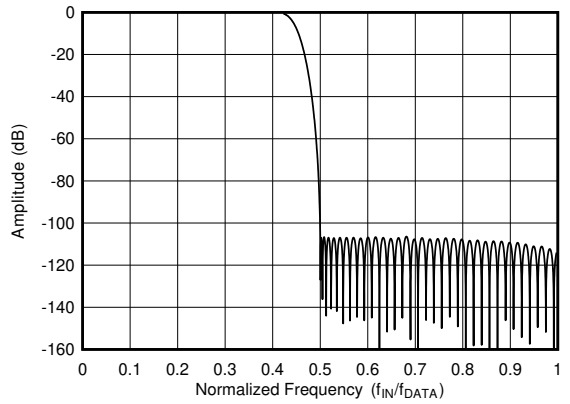

Figure 8-6. Wideband Filter Frequency Response

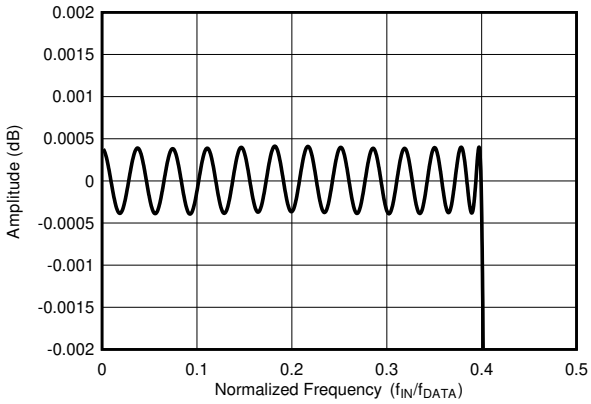

Figure 8-7. Wideband Filter Passband Ripple

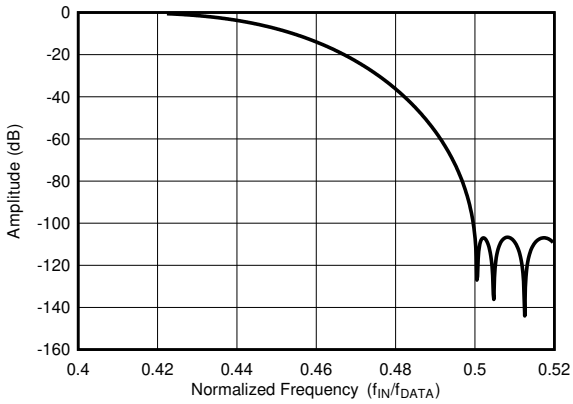

Figure 8-8. Wideband Filter Transition Band

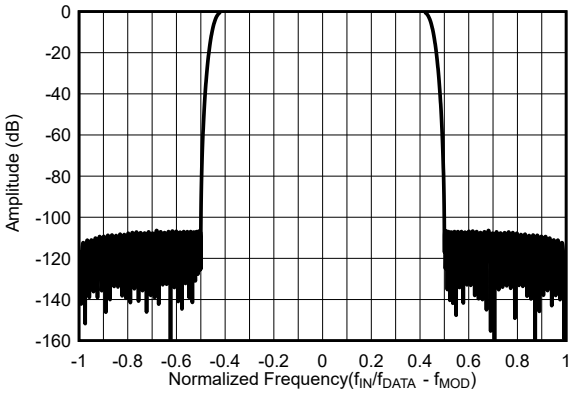

Figure 8-9. Wideband Filter Frequency Response Centered at f_{MOD}

The group delay of the filter is the time for an input signal to propagate through the filter. Because the filter is a linear-phase design, the envelope of a complex input signal is undistorted by the filter. The group delay (expressed in units of time) is constant versus frequency with a fixed value = $34/f_{DATA}$. After a step input is applied, fully settled data is provided at 68 data periods. The filter group delay ($34/f_{DATA}$) and the step input settling time ($68/f_{DATA}$) are shown in Figure 8-10.

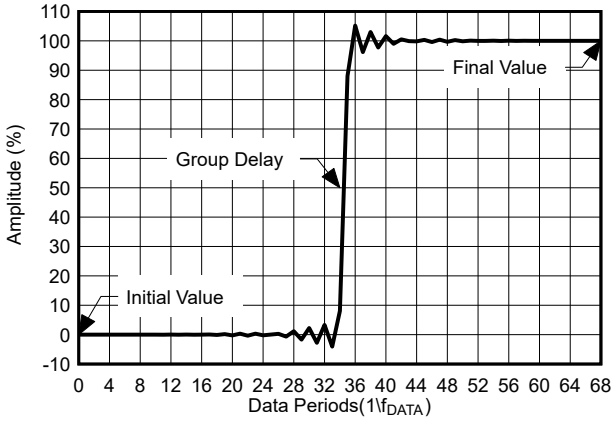

Figure 8-10. Wideband Filter Input Step Response

When the device is synchronized, the first 68 conversion periods are internally suppressed until the filter is settled. There is no need to discard data after synchronization. Conversion latency time is shown in *latency time* column of Table 8-2. An additional 0.4 µs is needed for filter overhead for all data rates. If a step input occurs unsynchronized to the conversion period, then add one conversion period to the settling time (69 conversions total) for fully settled data.

Table 8-2. Wideband Filter

OSR	DATA RATE (kSPS)	–0.1-dB FREQUENCY (kHz)	–3-dB FREQUENCY (kHz)	LATENCY TIME (µs)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)				
32	400	165	174.96	170.4
64	200	82.5	87.48	340.4
128	100	41.25	43..74	680.4
256	50	20.625	21.87	1360.4
512	25	10.312	10.935	2720.4
1024	12.5	5.156	5.467	5440.4
2014	6.25	2.578	2.734	10880.4
4096	3.125	1.289	1.367	21760.4
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)				
32	50	20.625	21.87	1363.1
64	25	10.312	10.935	2723.1
128	12.5	5.156	5.467	5443.1
256	6.25	2.578	2.734	10883.1
512	3.125	1.289	1.37	21763.1
1024	1.5625	0.645	0.683	43523.1
2048	0.78125	0.322	0.342	87043.1
4096	0.390625	0.161	0.171	174083.1

8.3.4.2 Low-Latency Filter (Sinc)

The low-latency filter is a sinc topology that minimizes the propagation time (latency) of the data through the filter. The latency time is short compared to the wideband filter, but the wideband filter possesses superior frequency characteristics. The device provides the choice of four configurations: sinc4, sinc4 + sinc1, sinc3 and sinc3 + sinc1.

Latency is defined as the time from the rising edge of START input, or setting the START bit, to the first falling edge of $\overline{DRDY}$. This is when fully settled data is available. There is no need to discard data because the intermediate conversions are suppressed by the ADC. The general expression of latency time is given by n ·

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f_{DATA} plus a fixed time for filter overhead, where n is the order of the sinc filter. Detailed latency times are shown in Table 8-3 through Table 8-6.

If the input is changed without using the START pin or START bit synchronize, then the next conversion results are partially-settled data. If an unsynchronized step input occurs, the number of conversions required to produce fully settled data is found by rounding the latency time value to the next integer and by adding one conversion period.

Equation 5 is the general expression of the sinc filter frequency response. For two-stage sinc filters (for example sinc3 + sinc1), the total frequency response is the multiplication of the individual sinc3 and sinc1 stages.

$$\left|H_{(f)}\right| = \left| \frac{\sin\left[\frac{A\pi f}{f_{CLKIN}}\right]}{A\sin\left[\frac{\pi f}{f_{CLKIN}}\right]} \right|^{n} \quad (5)$$

where

- f = signal frequency
- A = OSR
- f_{CLKIN}: f_{MOD} (stage 1), f_{MOD}/A (stage 2)
  - f_{MOD} = 12.8 MHz for high-speed mode, 1.6 MHz for low-speed mode
- n = order of the sinc filter (1, 3 or 4)

8.3.4.2.1 Sinc4 Filter

The sinc4 filter averages and down-samples the modulator data to yield data rates ranging from 1066.6 kSPS to 3.125 kSPS in high-speed mode and data rates ranging from 133.333 kSPS to 0.390625 kSPS in low-speed mode. Increasing the OSR decreases data rate while simultaneously reducing signal bandwidth and total noise due to increased decimation and increased data averaging. Table 8-3 shows the sinc4 filter characteristics.

Table 8-3. Sinc4 Filter Characteristics

OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)	LATENCY TIME (µs)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)			
12	1066.666	242.666	4.38
16	800	182	5.63
24	533.333	121.333	8.13
32	400	91.0	10.63
64	200	45.5	20.63
128	100	22.75	40.63
256	50	11.375	80.63
512	25	5.687	160.63
1024	12.5	2.844	320.63
2048	6.25	1.422	640.63
4096	3.125	0.711	1280.63
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)			
12	133.333	30.333	35.04
16	100	22.75	45.04
24	66.666	15.166	65.04
32	50	11.375	85.04
64	25	5.687	165.04
128	12.5	2.844	325.04
256	6.25	1.422	645.04

Table 8-3. Sinc4 Filter Characteristics (continued)

OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)	LATENCY TIME (µs)
512	3.125	0.711	1445.04
1024	1.5625	0.355	2565.04
2048	0.78125	0.177	5125.04
4096	0.390625	0.089	10245.04

Figure 8-11 and Figure 8-12 show the frequency response of the sinc4 filter for OSR = 32. The frequency response consists of a series of amplitude nulls occurring at discrete frequencies. The null frequencies occur at multiples of f_{DATA}. At the null frequencies, the filter has zero gain. An image of the frequency response repeats at multiples of f_{MOD}, as shown in Figure 8-12. No attenuation is provided by the filter at input frequencies near $n \cdot f_{MOD}$ (n = 1, 2, 3, and so on), and if present, will alias into the passband.

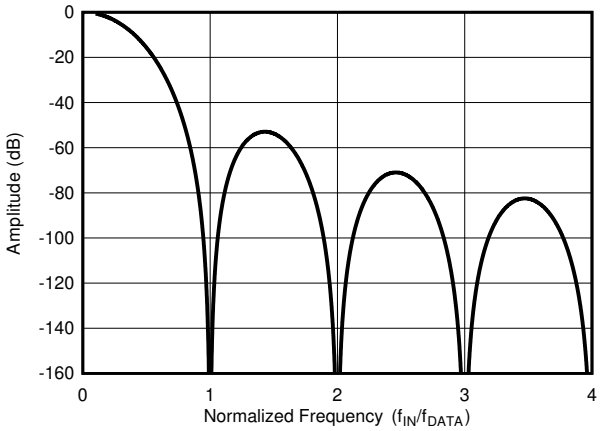

Figure 8-11. Sinc4 Frequency Response (OSR = 32)

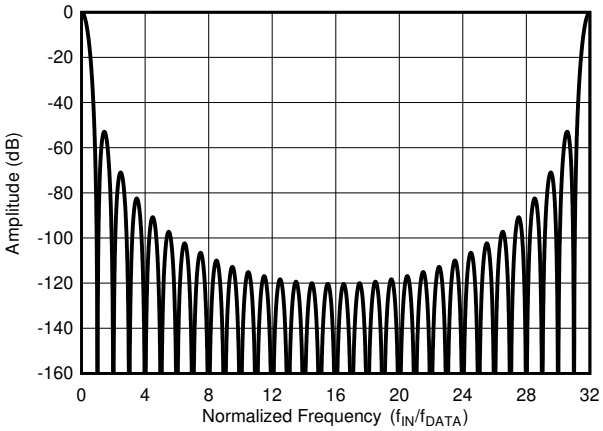

Figure 8-12. Sinc4 Frequency Response to f_{MOD} (OSR = 32)

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8.3.4.2.2 Sinc4 + Sinc1 Filter

The sinc4 + sinc1 filter is the cascade of two filter sections: sinc4 + sinc1. In this filter mode, the OSR of the sinc4 stage is fixed at 32 while the OSR of the sinc1 stage determines the output data rate. The sinc4 + sinc1 filter mode has comparably less latency time compared to the single-stage sinc4 filter. Table 8-4 summarizes the sinc4 + sinc1 filter characteristics.

Table 8-4. Sinc4 + Sinc1 Filter Characteristics

SINC4 OSR	SINC1 OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)	LATENCY TIME (µs)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)				
32	2	200	68.35	13.13
32	4	100	40.97	18.13
32	10	40	17.47	33.13
32	20	20	8.814	58.13
32	40	10	4.420	108.13
32	100	4	1.770	258.13
32	200	2	0.885	508.13
32	400	1	0.442	1008.13
32	1000	0.4	0.177	2508.13

Table 8-4. Sinc4 + Sinc1 Filter Characteristics (continued)

SINC4 OSR	SINC1 OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)	LATENCY TIME (µs)
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)				
32	2	25	8.544	105.04
32	4	12.5	5.121	145.04
32	10	5	2.184	265.04
32	20	2.5	1.102	465.04
32	40	1.25	0.552	865.04
32	100	0.5	0.221	2065.04
32	200	0.25	0.111	4065.04
32	400	0.125	0.055	8065.04
32	1000	0.05	0.022	20065.04

Figure 8-13 shows the frequency response of the sinc4 + sinc1 filter for three values of OSR. The combined frequency response is the overlay of the sinc1 filter with the sinc4 filter. For low values of OSR, the response profile is dominated by the roll-off of the sinc4 filter. Nulls in the frequency response occur at n · f_{DATA}, n = 1, 2, 3 and so on. At the null frequencies, the filter has zero gain.

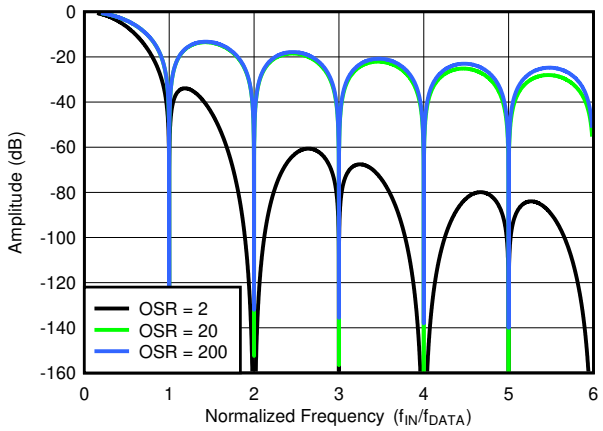

Figure 8-13. Sinc4 + Sinc1 Frequency Response

8.3.4.2.3 Sinc3 Filter

The sinc3 filter mode is a single stage filter. Relatively high values of OSR yield key data rates of 480 SPS, 400 SPS, 60 SPS and 50 SPS. Due to the large width of the frequency response notch, excellent NMRR and CMRR are achieved by rejecting line-frequency noise. Table 8-5 summarizes the characteristics of the sinc3 filter.

Table 8-5. Sinc3 Filter Characteristics

OSR	DATA RATE (SPS)	–3-dB FREQUENCY (Hz)	LATENCY (ms)	REJECTION OF FIRST NULL (dB)	
				2% CLOCK TOLERANCE	6% CLOCK TOLERANCE
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)					
26667	480	126	6.25	100	71
32000	400	105	7.50	100	71
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)					
26667	60	15.7	50.01	100	71
32000	50	13.1	60.01	100	71

Figure 8-14 shows the frequency response of the sinc3 filter (OSR = 32000). Figure 8-15 shows the detailed response in the region of 0.9 to 1.1 · f_{IN}/f_{DATA}.

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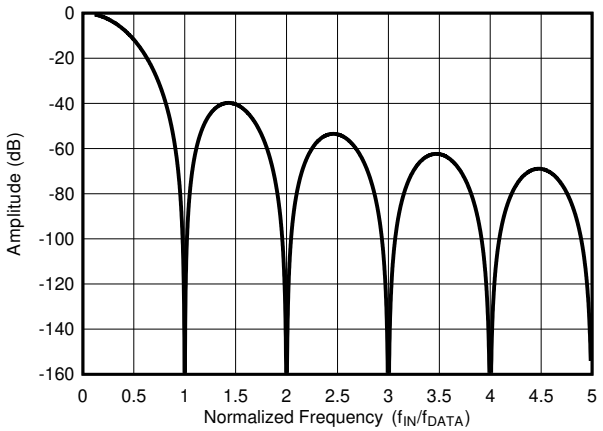

Figure 8-14. Sinc3 Frequency Response (OSR 32000)

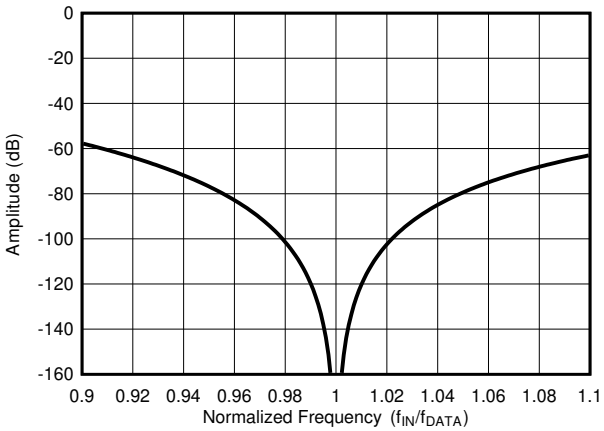

Figure 8-15. Detail Sinc3 Frequency Response (OSR 32000)

8.3.4.2.4 Sinc3 + Sinc1 Filter

The sinc3 + sinc1 filter mode is the cascade of the sinc3 and sinc1 filters. The OSR of sinc3 stage is fixed (32000) and the OSR of the sinc1 stage is programmable to 3 and 5. Table 8-6 summarizes the characteristics of the sinc3 + sinc1 filter.

Table 8-6. Sinc3 + Sinc1 Filter Characteristics

SINC3 OSR	SINC1 OSR	DATA RATE (SPS)	–3-dB FREQUENCY (HZ)	LATENCY (ms)	REJECTION OF FIRST NULL (dB)	
					2% CLOCK TOLERANCE	6% CLOCK TOLERANCE
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)						
32000	3	133.3	54	12.5	37	26
32000	5	80	34	17.5	37	26
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)						
32000	3	16.7	6.7	100.1	34	26
32000	5	10	4.2	140.01	34	26

Figure 8-16 shows the frequency response of the sinc3 + sinc1 filter. The frequency response exhibits the characteristic sinc filter response lobes and nulls. The nulls occur at f_{DATA} and at multiples thereof. Figure 8-17 shows the detailed response in the region of 0.9 to 1.1 · f_{IN}/f_{DATA}.

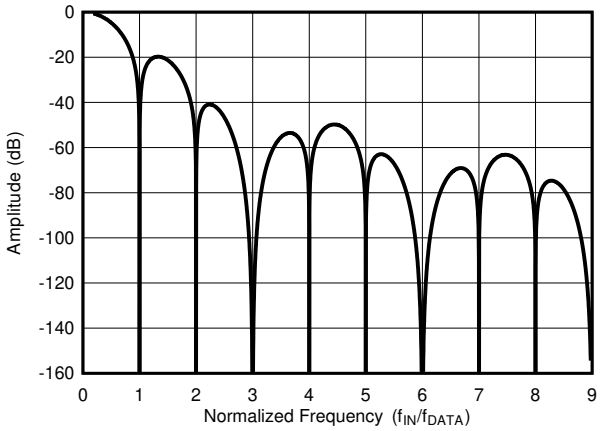

Figure 8-16. Sinc3 + Sinc1 Frequency Response

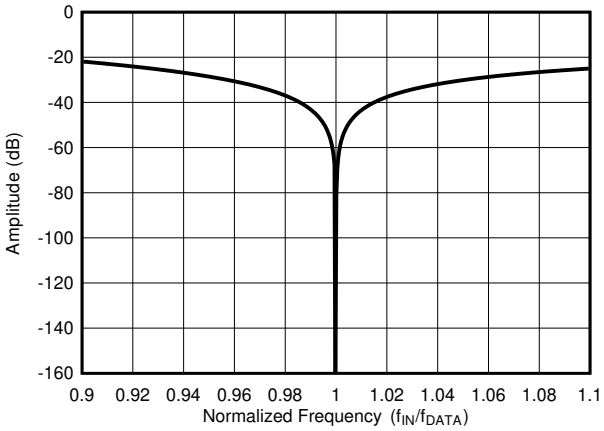

Figure 8-17. Detail Sinc3 + Sinc1 Frequency Response

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8.3.5 VCM Output Voltage

The device provides a buffered output voltage on the VCM pin equal to the midpoint voltage of AVDD1 – AVSS. The VCM output is intended to drive the output common-mode voltage (OCMV) of a full differential amplifier (FDA) or to level-shift the input of amplifier stages by driving the amplifier's non-inverting pin. The OCMV control input of many FDA drivers default to a mid-supply level when floated. Therefore, connection to the VCM output pin of the FDA is optional because the same functionality is provided within the FDA.

See the Electrical Characteristics for the resistive and capacitive load specifications for the VCM output. The VCM output is enabled by the VCM bit of the CONFIG1 Register.

8.3.6 Power Supplies

The device has three analog power supplies (AVDD1, AVSS, AVDD2) and one digital power supply (IOVDD). The power supplies can be sequenced in any order and are tolerant to slow or fast power supply voltage ramp rates. However, in no case must any analog or digital input exceed the respective AVDD1 and AVSS (analog) or IOVDD (digital) power supply, as specified in the Recommended Operating Conditions .

8.3.6.1 AVDD1 and AVSS

Analog power supplies AVDD1 and AVSS are used to power the input buffers and the sampling switches within the modulator. AVDD1 and AVSS can either be configured as bipolar supplies, such as ±2.5 V, or unipolar supplies, such as AVDD1 = 5 V and AVSS = DGND. Selection of bipolar or unipolar supply configuration determines the type of input signal measured by the ADC: bipolar or unipolar. Use a parallel combination of 1-µF and 0.1-µF supply bypass capacitors across the AVDD1 and AVSS supply pins with a 3-Ω series resistor between the bypass capacitors and the AVDD1 pin of the device. Place the resistor as close as possible to the AVDD1 pin. See the Recommended Operating Conditions for the specification of AVDD1 and AVSS.

8.3.6.2 AVDD2

Analog power supply voltage AVDD2 powers the ADC's modulator. AVDD2 and AVDD1 can be connected together to simplify the power supply design, or AVDD2 can be operated by a separate, low voltage supply to reduce device power consumption. Be aware the AVDD2 supply voltage is with respect to AVSS. Use a combination of 1-µF and 0.1-µF bypass capacitors across the AVDD2 and AVSS supply pins. See the Recommended Operating Conditions for the rating of AVDD2.

Table 8-7 shows examples of AVDD1, AVSS and AVDD2 power supply configurations.

Table 8-7. AVDD1, AVSS and AVDD2 Power Supply Combinations (High speed mode, Nominal values, Voltages with respect to DGND)

CONFIGURATION	AVDD1	AVSS	AVDD2
Unipolar supply	5 V	0 V	5 V
Unipolar supply, low power consumption	5 V	0 V	1.8 V
Bipolar supply	2.5 V	–2.5 V	2.5 V
Bipolar supply, low power consumption	2.5 V	–2.5 V	0 V

8.3.6.3 IOVDD

IOVDD is the digital I/O supply voltage for the device. The IOVDD voltage is internally regulated to 1.25 V to power the digital logic. Bypass IOVDD to DGND with a parallel combination of 1-µF and 0.1-µF capacitors. See the Recommended Operating Conditions for the rating of IOVDD. The voltage level of IOVDD is independent of the analog supply configuration.

8.3.6.4 CAPA and CAPD

CAPA and CAPD are the voltage outputs of internal analog and digital voltage regulators. CAPA is the analog regulator output used to power the modulator from the AVDD2 power supply. The regulator output is 1.6 V with respect to AVSS. Bypass the CAPA pin with a 1-µF capacitor to AVSS. CAPD is the digital regulator output used to power the digital section from the IOVDD supply. The regulator output is 1.25 V with respect to DGND. Bypass with a 1-µF capacitor across CAPD to DGND. Place no external loads on either of these pins.

8.4 Device Functional Modes

8.4.1 Power-Scalable Operating Modes

The ADC offers the option of two power-scalable operating modes that affect power consumption and the available range of data rate speeds: high speed and low speed. The modes optimize between signal bandwidth, data rate and power consumption. High-speed mode provides greater signal bandwidth and data rate, while the low-speed mode reduces device power consumption for applications not requiring large signal bandwidths. The input clock frequency must be adapted to the mode. For high-speed mode, the nominal clock is 25.6 MHz and for low-speed mode, the nominal clock is 3.2 MHz (see the ADC Clock section for details). The speed mode is programmed by the SPEED_MODE bit in the CONFIG2 register.

8.4.2 Idle Mode

When conversions are stopped, the ADC can be programmed to either remain fully powered (idle mode) or enter a low-power standby mode. In idle mode, the input and reference buffer remain powered and the modulator continues sampling the signal and the reference voltage inputs. Only the digital filter is disabled when conversions are stopped. When conversions are started, the digital filter is enabled to begin conversions. The mode is programmed by STBY_MODE bit of register CONFIG2.

8.4.3 Standby Mode

When conversions are stopped, the device has the option to enter a low-power standby mode. When programmed, standby mode automatically engages when conversions are stopped. Power consumption reduces substantially but not to the level provided in the power-down mode. Sampling of the signal and reference voltage inputs are stopped in standby mode. When conversions are subsequently restarted by the user, the first conversion is delayed an additional 24 clock cycles to stabilize modulator operation. Program the STBY_MODE bit of register CONFIG2 to select standby mode.

8.4.4 Power-Down Mode

The device is placed in a full power-down mode by setting the PWDN bit of the CONFIG2 register. In power-down mode, the analog and digital sections are powered-off except for the SPI, in order to maintain device communications to exit power-down mode through the SPI. The digital LDO remains active in order to maintain user register settings. The sampling of the signal input and reference inputs are stopped. Exit the power-down mode by writing 0b to the PWDN bit or by resetting the device.

8.4.5 Reset

Resetting the ADC involves reset of the digital logic, the SPI, and the user registers to the default values. The ADC is reset using three methods: automatic reset at power-on (POR), reset using the $\overline{\text{RESET}}$ pin and reset via SPI. See Figure 6-3 for when the ADC is available for operation after reset.

8.4.5.1 Power-On Reset (POR)

The ADC uses power-supply monitors to detect power-on and brownout conditions. Power-on or power-cycling of the IOVDD digital supply results in device reset. Power-on or power-cycling of the analog power supplies does not reset the device.

Figure 8-18 shows the voltage thresholds for IOVDD and the CAPD voltage. The monitors are ANDed to release the internal reset state. After IOVDD power-up, the SPI of the ADC is ready for communication when $\overline{\text{DRDY}}$ transitions high. If START is high, $\overline{\text{DRDY}}$ subsequently drives low to indicate completion of the first conversion. However, valid ADC conversions are only possible when all analog and digital power supplies are within the recommended voltage range. The POR_FLAG bit of the STATUS register sets to indicate an ADC reset. Write 1b to clear the bit in order to detect the next POR event. Because a low voltage on IOVDD internally resets the analog LDO, the ALV_FLAG (analog low voltage flag) triggers with the POR_FLAG regardless of the analog power supply.

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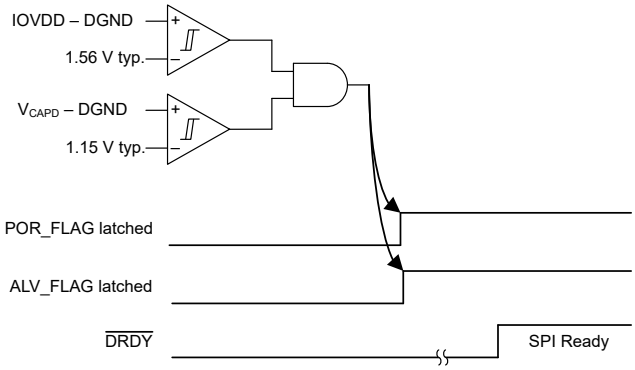

Figure 8-18. Digital Supply Threshold

Figure 8-19 shows the thresholds for the analog supplies. Four analog supply voltages (AVDD1 – DGND), (AVDD1 – AVSS), (AVDD2 – AVSS) and the CAPA voltage are monitored. These monitors detect analog supply low-voltage and brown-out conditions. Valid ADC conversions are only possible when all analog and digital power supplies are within the recommended voltage range. The ALV_FLAG of the STATUS register sets when any analog voltage is below the respective threshold. Write 1b to clear the bit to detect the next analog supply low-voltage event. Power cycling the analog power supplies does not result in device reset.

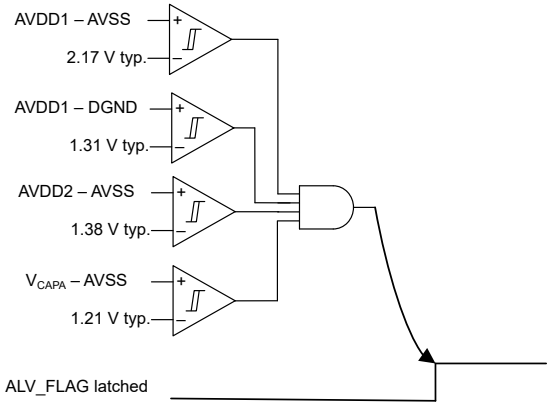

Figure 8-19. Analog Supply Threshold

8.4.5.2 RESET Pin

The device is reset by toggling the RESET pin low to high. The RESET pin is a Schmidt-triggered input to reduce noise. The pin integrates a 20-kΩ pull-up resistor as shown in Figure 8-20. See Figure 6-3 for RESET input timing requirements and when SPI communication can be initiated after reset. Because the ADC has a power-on reset circuit, it is not necessary to perform reset after power on.

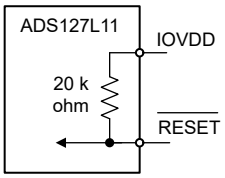

Figure 8-20. RESET Input

8.4.5.3 Reset by SPI Register Write

The device is reset through the SPI by writing 01011000b to the CONTROL register. Writing any other value does not reset the ADC. In 4-wire SPI mode, reset takes effect at the end of the SPI frame by driving CS high. In 3-wire SPI mode, reset takes effect on the last falling edge of SCLK of the register write operation. 3-wire

SPI mode requires that the SPI frame is already in synchronization with the SPI host. If this is not an assured condition, use the Reset by SPI Pattern option described in Reset by SPI Input Pattern to reset the device.

8.4.5.4 Reset by SPI Input Pattern

The device is reset through SPI though the option of two input patterns. Reset Option 1 is to input a minimum of 1023 consecutive ones followed by one zero (1024 clocks total). The device resets on the falling edge of SCLK when the final zero is shifted in. This pattern can be used in 3- or 4-wire SPI modes. See Figure 8-21 for an example pattern.

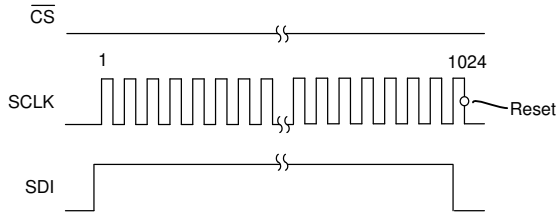

Figure 8-21. Reset Pattern (3-wire or 4-wire SPI Mode)

Reset option 2 is used in 4-wire SPI mode only. To reset, input a minimum of 1024 consecutive ones (no ending zero value), followed by taking $\overline{CS}$ high at which time reset occurs. Option 2 reset pattern is recommended in daisy-chain connected devices. See Figure 8-22 for an example pattern.

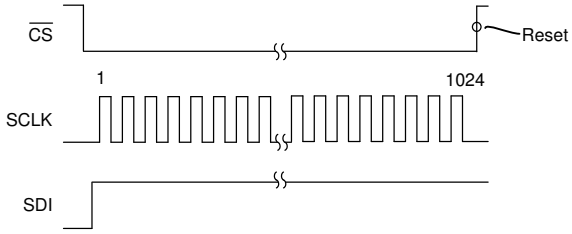

Figure 8-22. Reset Pattern (4-wire SPI Mode)

8.4.6 Conversion Control

Conversions are controlled and synchronized by the START pin or through SPI. If controlling conversions through SPI, keep the START pin low. Writing to any register from 04h through 0Eh results in conversion restart and loss of external synchronization. If necessary, resynchronize the ADC.

The ADC provides three conversion control modes: Synchronized, One-shot and Start/Stop mode, each with its own specific functionality. The mode is programmed by the START_MODE[1:0] bits of register CONFIG2 for details. Only the One-shot and Start/Stop modes can be controlled through SPI.

To allow for digital filter settling when a conversion is first started, the time for completion of the first conversion (latency time) is longer than the normal conversion period. The latency time depends on the filter mode and data rate (see the Digital Filter section for details).

8.4.6.1 Synchronized Control Mode

In the synchronized control mode, conversions are synchronized on the rising edge of the START pin. Both one-time synchronization and continuous synchronizing pulse inputs are accepted. After the initial synchronization, if the time to the next rising edge of START is an integer number of conversion periods, within a $\pm 1/f_{CLK}$ window, the ADC does not resynchronize. This is because the ADC is already in synchronization. Otherwise, the ADC resynchronizes at the rising edge of START. Applying continuous synchronizing pulse inputs results in resynchronization only when needed. Due to the delay of the digital filter, a time offset exists between the synchronizing input of START and the $\overline{DRDY}$ output. Figure 8-23 shows the operation of the START and $\overline{DRDY}$ pins when resynchronized. $\overline{DRDY}$ is forced high at the 8th edge of SCLK of the MSB conversion data byte or if data is not read, pulses high just before the next falling edge of $\overline{DRDY}$

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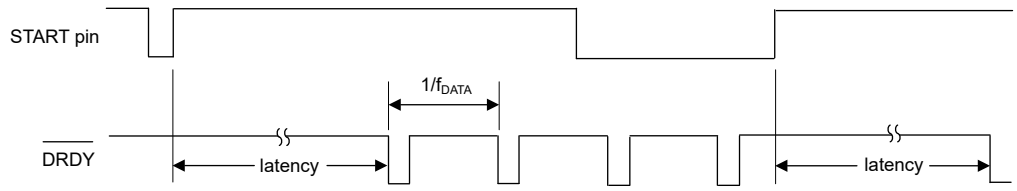

Figure 8-23. Synchronized Control Mode

8.4.6.2 Start/Stop Control Mode

Start/Stop mode controls (gates) the start and stop of conversions. Conversions are started by taking the START pin high or by writing 1b to the START bit of register CONTROL. Conversions continue until stopped by taking the START pin low or writing 1b to the STOP bit. $\overline{\text{DRDY}}$ is driven high at conversion start and is driven low each time the conversion data are available for readback. If START is taken low or 1b is written to the STOP bit during a conversion, that conversion will run to completion and then stop. (See Figure 6-4 for START timing). To restart the ongoing conversion, take the START pin low to high, or write 1b to the START bit a second time. Figure 8-24 shows the operation of the START and $\overline{\text{DRDY}}$ pins. In Standby mode, $\overline{\text{DRDY}}$ returns high 3 clock cycles after the low transition, otherwise $\overline{\text{DRDY}}$ is forced high at the 8th edge of SCLK of the MSB conversion data byte or if data is not read, pulses high just before the next falling edge of $\overline{\text{DRDY}}$.

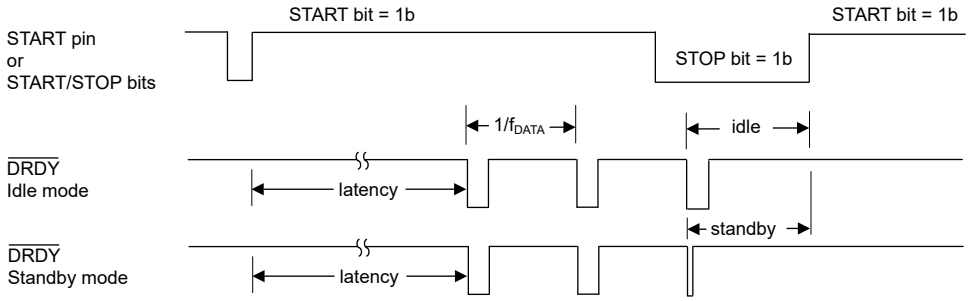

Figure 8-24. Start/Stop Control Mode

8.4.6.3 One-Shot Control Mode

In one-shot mode, the ADC performs one conversion when START is taken high, or when the START bit of the CONTROL register is set by the user. $\overline{\text{DRDY}}$ drives high to indicate the conversion is started and drives low when the conversion is complete. Data is available for readback at that time. After the first conversion completes, conversions are stopped. Taking START low, or writing 1b to the STOP bit does not interrupt the ongoing conversion. To restart the conversion, take START low to high, or write 1b to the START bit a second time. Figure 8-25 shows the operation of the START and $\overline{\text{DRDY}}$ pins in one-shot control mode. In Standby mode, $\overline{\text{DRDY}}$ returns high 3 clock cycles after the low transition, otherwise $\overline{\text{DRDY}}$ is forced high at the next rising edge of START.

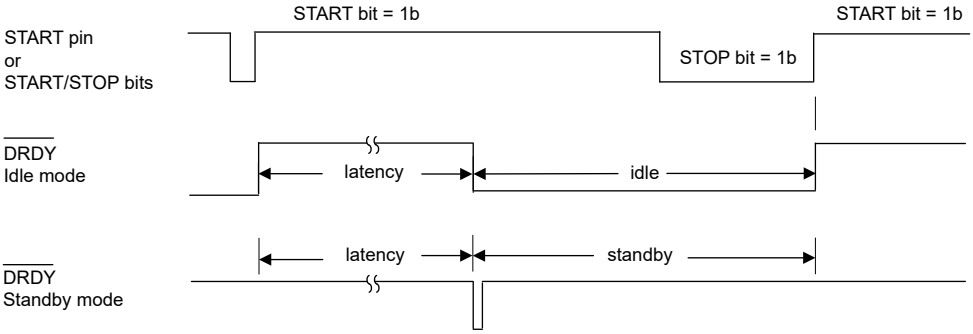

Figure 8-25. One-shot Control Mode

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8.4.7 Conversion-Start Delay Time

A time setting can be programed that delays the start of the internal filter cycle after the START pin or START bit is applied. The delay time setting allows for settling of external circuit components, such as after an external multiplexer input is changed. Subsequent (continuous) conversions do not use the delay time. The amount of delay time programed will increase the overall conversion latency time. See the DELAY[2:0] bits of register CONFIG3 for details.

8.4.8 Calibration

The ADS127L11 provides the ability to calibrate offset and gain error. Calibration consist of user programmable offset and gain registers. As shown in Figure 8-26, the 24-bit offset correction value is subtracted from the conversion data before multiplication by the 24-bit gain correction value. Output data is clipped to +FS and –FS code values. In 16-bit data format, data is rounded to 16 bits after calibration.

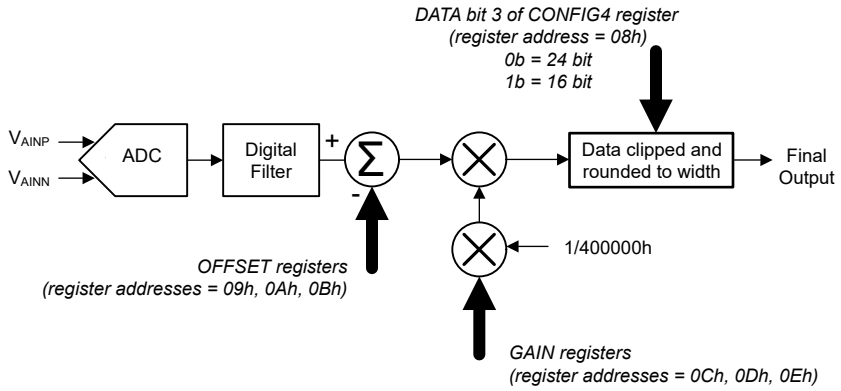

Figure 8-26. Calibration Block Diagram

Conversion data is calibrated as shown in Equation 6:

$$\text{Final Output Data} = (\text{Data} - \text{OFFSET}[2:0]) \times \text{GAIN}[2:0] / 400000\text{h} \quad (6)$$

8.4.8.1 Offset Calibration Registers (Addresses 09h, 0Ah, 0Bh)

The offset calibration value is 24 bits consisting of three 8-bit registers in two's-complement format. The offset value is subtracted from the conversion data. Register 09h is the most-significant byte, register 0Ah is the middle byte, and register 0Bh is the least-significant byte. If the ADC is programmed to 16-bit resolution, the least-significant offset byte provides sub-LSB resolution. Table 8-8 shows example offset values.

Table 8-8. Offset Calibration Values

OFFSET CALIBRATION VALUE	OFFSET APPLIED
000010h	–16 LSB
000001h	–1 LSB
FFFFFFh	1 LSB
FFFF00h	16 LSB

8.4.8.2 Gain Calibration Registers (Addresses 0Ch, 0Dh, 0Eh)

The gain calibration value is 24 bits consisting of three 8-bit registers in straight binary format, normalized to unity gain at 400000h. Register 0Ch is the most-significant byte, register 0Dh is the middle byte, and register 0Eh is the least-significant byte. For example, to correct gain errors > 1, the gain calibration values are < 400000h. Table 8-9 shows example gain calibration values.

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Table 8-9. Gain Calibration Values

GAIN CALIBRATION VALUE	GAIN APPLIED
433333h	1.05
400000h	1
3CCCCCh	0.95

8.4.8.3 Calibration Procedure

The recommended calibration procedure is as follows:

1. Preset the offset and gain calibration registers to 000000h and 400000h, respectively.
2. Perform offset calibration by shorting the inputs at the ADC or at the system level to include offset error of the input buffer stage. Acquire conversion data and write the average value of the data to the offset calibration registers. Averaging the data reduces conversion noise to improve calibration accuracy.
3. Perform gain calibration by applying a calibration signal at the ADC or at the system level to include the gain error of the input buffer stage. For standard input range mode, choose the calibration voltage less than the full-scale input range to avoid clipping the output code. Clipped output codes will cause inaccurate calibration. For example, use a 3.9-V calibration signal with V_{REF} = 4.096 V. For the extended input range mode, the calibration signal can be equal to V_{REF} without causing a clipped output code. Acquire conversion data and average the results. Calculate the gain calibration value using Equation 7.

$$\text{Full Scale Calibration Value} = (\text{expected output code}/\text{actual output code}) \cdot 400000\text{h} \quad (7)$$

For example, the expected output code using a 3.9-V calibration voltage operating with a 4.096-V reference voltage in the standard range is: (3.9/4.096)·7FFFFFh = 79E000h.

8.5 Programming

8.5.1 Serial Interface (SPI)

The serial interface is used to read conversion data, configure device registers, and control ADC conversions. The optional CRC mode validates error-free transmission of data between the host and ADC. A separate register map CRC is used to detect register map changes after the initial register data are loaded.

The serial interface consists of four lines: $\overline{CS}$, SCLK, SDI, and SDO/$\overline{DRDY}$. The serial interface operates in peripheral mode (passive) where SCLK is driven by the host. The interface is compatible to SPI Mode 1, where CPOL = 0 and CPHA = 1. In SPI Mode 1, SCLK idles low, data are updated on SCLK rising edges and data are read on SCLK falling edges. The interface supports full-duplex operation, meaning input data and output data can be transmitted simultaneously. The interface supports daisy-chain connection of multiple ADCs to simplify the SPI lines to four.

8.5.1.1 Chip Select ($\overline{CS}$)

$\overline{CS}$ is a Schmidt-trigger, active-low input that enables the interface for communication. A communication frame is started by taking $\overline{CS}$ low and is ended by taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the device ends the frame by interpreting the last 16 bits of input data (24 bits in CRC mode) regardless of the number of bits shifted in. When $\overline{CS}$ is high, the interface is reset, commands are blocked and SDO/ $\overline{DRDY}$ enters a high-impedance state. $\overline{DRDY}$ is an active output regardless of the state of $\overline{CS}$. $\overline{CS}$ can be tied low to operate the interface in 3-wire SPI mode.

8.5.1.2 Serial Clock (SCLK)

SCLK is the serial clock input to shift data into and out of the ADC. Output data are updated on the rising edge of SCLK and input data are latched on the falling edge of SCLK. SCLK is a Schmitt-triggered input designed to provide noise immunity. Even though SCLK is noise resistant, keep SCLK as noise-free as possible to avoid unintentional SCLK transitions. Avoid ringing and overshoot on the SCLK input. A series termination resistor at the SCLK driver can often reduce ringing.

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8.5.1.3 Serial Data Input (SDI)

SDI is the serial interface data input. SDI is used to load register data into the device. Input data are latched on the falling edge of SCLK. SDI is a Schmidt-triggered input designed to provide noise immunity.

8.5.1.4 Serial Data Output/Data Ready (SDO/$\overline{\text{DRDY}}$)

SDO/$\overline{\text{DRDY}}$ is a mode-programmable output pin. The programmable modes are data-output only mode, or dual-function operation of data output and data ready. Output data are updated on the rising edge of SCLK. The SDO/$\overline{\text{DRDY}}$ pin is in a high-Z state when $\overline{\text{CS}}$ is high. The dual function mode multiplexes data output and the DRDY functions onto a single pin. See the Hardware Method section of data ready detection for details of dual-function mode operation. The SDO_MODE bit of register CONFIG2 programs the mode. In order to operate ADCs in daisy-chain mode, the data-output only mode must be used.

8.5.2 Data Frame

Communication through the serial interface is based on the concept of data frames. A data frame consists of a prescribed number of SCLKs needed to shift-in or shift-out data. A frame is started by taking $\overline{\text{CS}}$ low and is ended by taking $\overline{\text{CS}}$ high. When $\overline{\text{CS}}$ is taken high, the device interprets the last 16 bits (or 24 bits in CRC mode) of input data regardless of the amount of data shifted into the device. In typical use, the input frame is sized to match the output frame size by padding the frame with leading zero-value bytes. However, if not transmitting and receiving data in full-duplex mode, the input command data can be optionally sized at the minimum value 16 bits (or 24 bits in CRC mode). The output frame size depends on the configuration of data resolution (16 or 24 bits), optional STATUS header and CRC bytes, as shown in Table 8-10. In 3-wire SPI mode, the input frame must always match the size of the output frame.

Table 8-10. Output Frame Size

DATA MODE	STATUS BYTE	CRC BYTE	FRAME SIZE
24 bit	no	no	24 bits
		yes	32 bits
	yes	no	32 bits
		yes	40 bits
16 bit	no	no	16 bits
		yes	24 bits
	yes	no	24 bits
		yes	32 bits

8.5.3 SPI CRC

The SPI Cyclic Redundancy Check (CRC) is an optional SPI communication error check used to detect transmission errors to and from the host. A CRC byte is transmitted with the input data by the host and a CRC byte is transmitted with the output data by the ADC. CRC for communications error check is enabled by the SPI_CRC bit of the CONFIG4 register.

The CRC input byte is calculated by the host on the two command bytes. Any input bytes padded to the start of the frame are not included in the CRC. The device checks the input command CRC against an internal calculation. If the CRC values do not match, the command is not executed and the SPI_ERR bit is set in the STATUS byte. Further register write operations are blocked except to the STATUS register to allow clearing the error by writing 1b to the SPI_ERR bit. Register read operations are not blocked unless SPI_CRC error is detected in the immediately preceding command.

The number of bytes used to calculate the output CRC depends on the amount of data transmitted in the frame. All output bytes that precede the output CRC are used in the CRC calculation. The number of bytes used for the output CRC calculation are summarized in Table 8-11.

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Table 8-11. Bytes Used for Output CRC Byte Calculation

CRC BYTE ARGUMENT	BYTE DESCRIPTION
2	16-bit resolution conversion data
	One byte of register data + 00h pad byte
3	24-bit resolution conversion data
	16-bit resolution conversion data + STATUS byte
	One byte of register data + two 00h pad bytes
4	24-bit resolution conversion data + STATUS byte
	One byte of register data + three 00h pad bytes

The CRC byte is the 8-bit remainder of the bitwise exclusive-OR (XOR) operation of the variable length argument by the CRC polynomial. The CRC is based on the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X^1 + 1$. The nine coefficients of the polynomial are: 100000111. The CRC calculation is initialized to all 1s to detect errors in the event that SDI and SDO/ $\overline{\text{DRDY}}$ have either failed low or failed high.

See the *ADS125H02 Design Calculator* software to calculate CRC values.

8.5.4 Full-Duplex Operation

The serial interface supports full-duplex operation. Full-duplex operation is the simultaneous transmission and reception of data in the same frame. For example, the register read command for the next register can be sent at the same time the previous register data are transmitted. Full duplex operation doubles the register read throughput when reading a sequence of registers. An example of full duplex operation is shown in Figure 8-28.

8.5.5 Device Commands

Commands are used to read and write data to the registers. The register map of Table 8-14 consists of a series of one-byte registers, accessible through read and write operations. The minimum frame length of the input command is two bytes (three bytes in SPI-CRC mode) and is interpreted at the end of the data frame. Table 8-12 shows the device commands for the ADS127L11.

Table 8-12. Interface Commands

DESCRIPTION	BYTE1	BYTE2	BYTE 3 (Optional CRC Byte)
No-Operation	00h	00h	D7h
Read Register Data	40h + address [3:0]	don't care	CRC of byte1 and byte2
Write Register Data	80h + address [3:0]	register data	CRC of byte1 and byte2
Reset Input Pattern	See Reset by SPI Input Patternand 3-Wire SPI Mode Reset sections for details		

8.5.5.1 No-Operation

The command bytes for no-operation are 00h, 00h. If SPI CRC mode is enabled for the interface (SPI_CRC = 1b), the third byte for the CRC is required. The CRC is computed over the two 00h input bytes, resulting in CRC = D7h. SDI can be held low during data readback, but if CRC mode is enabled the SPI_ERR flag will set, blocking register write operations. The SPI_ERR flag can be ignored while reading conversion data until which time it is desired to write to registers. Then the SPI_ERR flag of the Status register must be cleared by writing 1b to enable register writes.

8.5.5.2 Read Register Command

The read register command is used to read data from a given register. The command follows an off-frame protocol where the read command is sent in one frame and the ADC responds with register data in the next frame. The register data output is most-significant-bit first. The first byte of the command is the base command value (40h) added to a 4-bit register address. The value of the second command byte is arbitrary, but is used with the first byte for the CRC calculation. The response to registers outside the valid address range is 00h.

Figure 8-27 shows an example of a 16-bit minimum frame size to read register data (16-bit data resolution, without STATUS and without CRC). Frame 1 is the command input frame and frame 2 is the register data output frame. The frames are delimited by taking $\overline{\text{CS}}$ high. The output data frame is padded with 00h after the register

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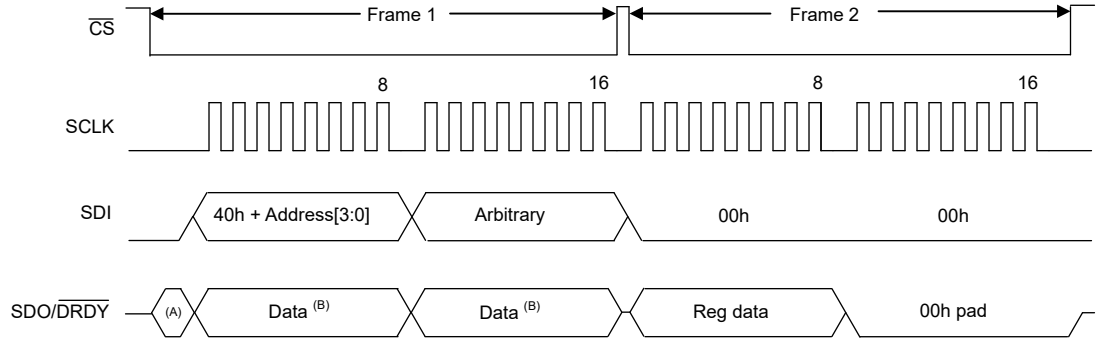
data byte to fill out the 16-bit frame. For 24-bit data, two 00h pad bytes are used in the output frame. One pad byte should be prefixed to the input frame if reading *conversion* data in optional full-duplex operation in frame 1. The output data frame can be shortened after reading the register data byte by taking $\overline{CS}$ high, but not in full-duplex operation. The option of full-duplex operation doubles the throughput of reading register data by the input of the next read register command during the output frame of the previous register (not shown).

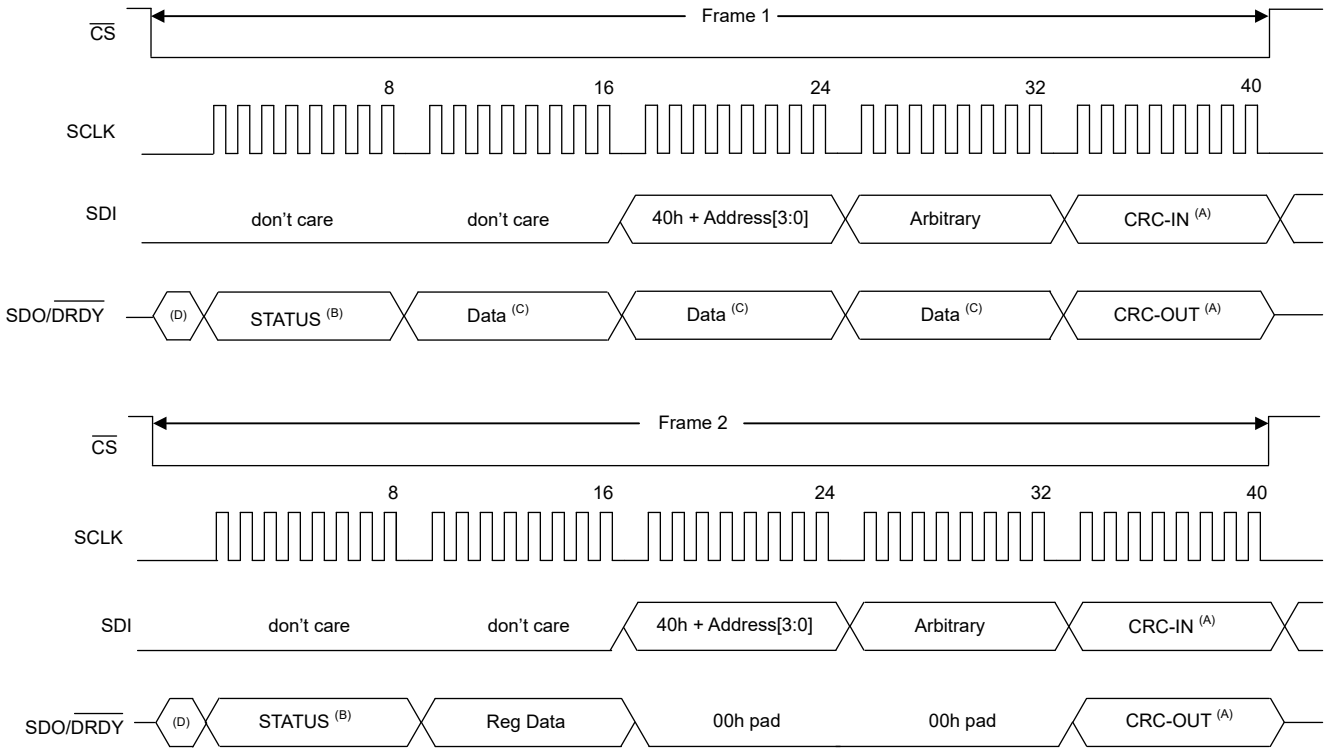


A. Previous state of SDO/ $\overline{DRDY}$ before first SCLK

B. Data is either 16 bits of conversion data, or if the read register command sent in prior frame then data = resister data + 00h,

Figure 8-27. Read Register Data, Minimum Frame Size (16-bit Data, No CRC or Output Header Bytes)

Figure 8-28 shows an example of a maximum frame size, read register operation. This example sends the read register command at the same time reading conversion data (full duplex operation). In frame 1, conversion data is output if the previous frame was not a read register command. The input command is prefixed with two don't care bytes in order to match the length of the output data frame. The prefixed input bytes are excluded from the CRC-IN byte, using only the values of the command byte and the arbitrary byte. The output CRC byte (CRC-OUT) includes all preceding bytes within the frame. Frame 2 outputs the register data with added zeros after the register data to position the CRC-OUT byte of the register data in the same location as the conversion data output of frame 1 (if frame 1 was not preceded by a read register command). If not previously set, the SPI_ERR bit of the STATUS header indicates whether the read register command was accepted.



A. Optional CRC byte. If CRC disabled, the frame shortens by one byte

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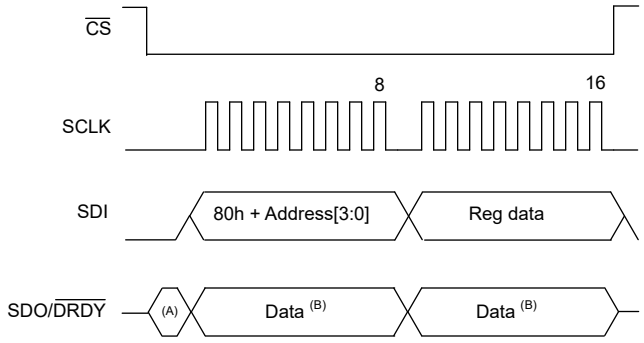
B. Optional STATUS byte. If STATUS disabled, the frame shortens by one byte
C. Depending on previous operation, data is either conversion data or register data + two 00h pad bytes
D. Previous state of SDO/ $\overline{DRDY}$ before first SCLK

Figure 8-28. Read Register Data, Maximum Frame Size (24-bit Data, Header and CRC bytes, Full-Duplex Operation)

8.5.5.3 Write Register Command

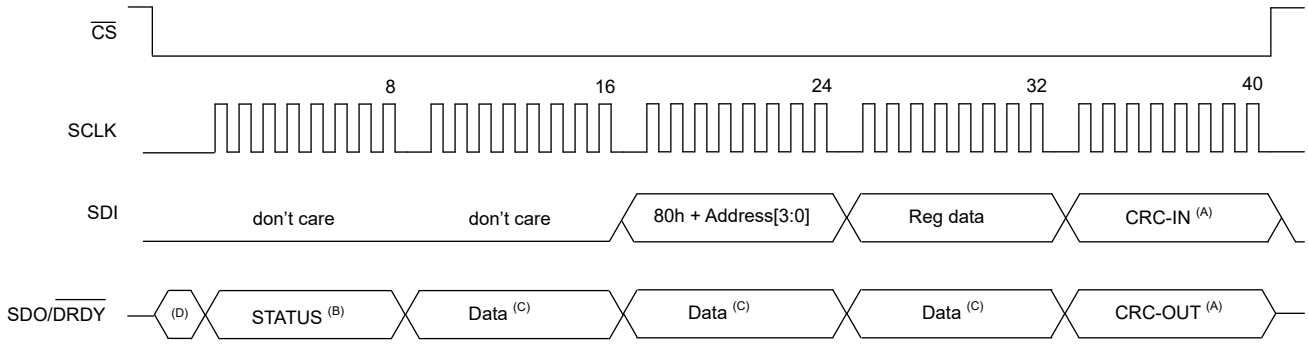
The write register command is used to write data to a given register. The write register operation is performed in one frame. The first byte of the command is the base value (80h) added to a 4-bit register address. The second byte of the command is the register data. Writing to registers outside the valid address range are ignored. Figure 8-29 shows an example of a register write operation with the minimum 16-bit frame size. For 24-bit resolution, the frame size should be three bytes in order to read conversion data in full-duplex mode (simultaneous data transmission and reception).



A. Previous state of SDO/ $\overline{DRDY}$ before first SCLK
B. Data is either the conversion data, or if the read register command was sent in prior frame, the data field is register data followed by 00h pad byte

Figure 8-29. Write Register Data, Minimum Frame Size (16-bit Data, No CRC or Output Header Bytes)

Figure 8-30 shows an example of a maximum frame size, write register operation. This example illustrates the option of full duplex operation for simultaneous transmission and reception of data. The input frame is prefixed with two don't care bytes to make the input the same length as the output so all output bytes can be transmitted Optional CRC and STATUS bytes are shown. Successful write operations can be verified by readback of the register data, or by checking the SPI_ERR bit of the STATUS byte for input communication errors. If an SPI input error occurred, SPI_ERR is set and further register write operations are disabled until reset by writing 1b to the bit.



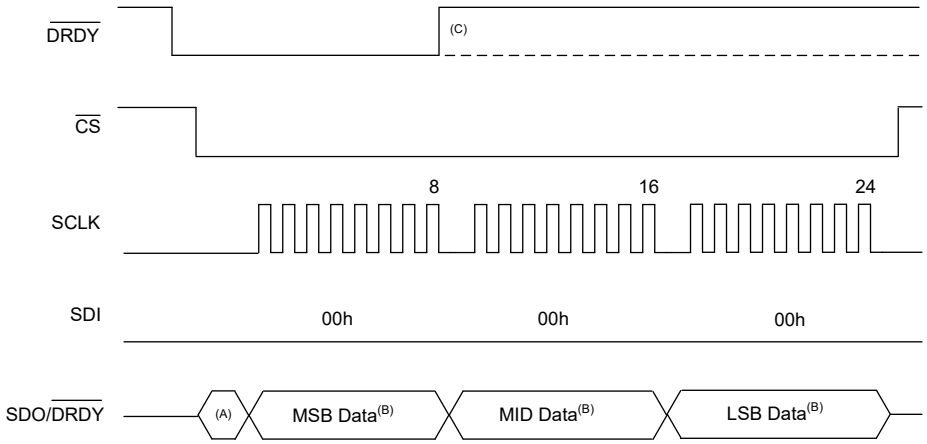
A. Optional CRC byte. If CRC disabled, the frame shortens by one byte
B. Optional STATUS byte. If STATUS disabled, the frame shortens by one byte
C. Data is either the 24-bit conversion data, or if the read register command was sent in the prior frame, data is register data followed by two 00h pad bytes
D. Previous state of SDO/ $\overline{DRDY}$ before the first SCLK

Figure 8-30. Write Register Data, Maximum Frame size (24-bit Data, Header and CRC bytes)

8.5.6 Read Conversion Data

To read conversion data, wait for $\overline{DRDY}$ to transition low, take $\overline{CS}$ low and begin applying SCLK to read the data (no command is used). If the register read command was sent in the previous frame then register data replaces conversion data. Conversion data is buffered making it available to read until one f_{MOD} before the next $\overline{DRDY}$ low transition. Conversion data may be read multiple times before the next conversion data are ready.

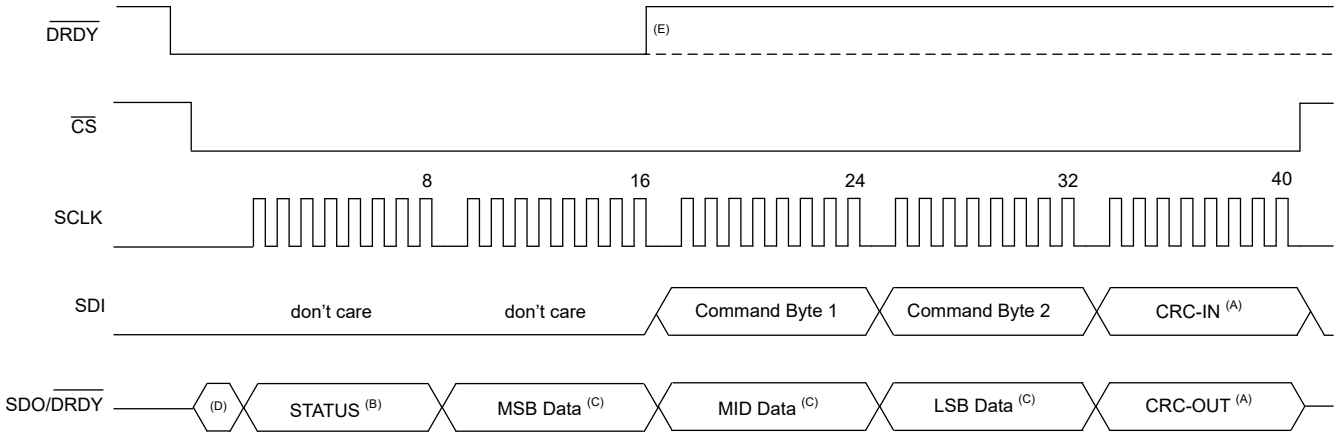
Figure 8-31 shows an example of reading conversion data in a minimum 24-bit format. The read operation is shown with the STATUS header and CRC bytes disabled. The 16-bit data option shortens the read operation to16 bits.



A. When SDO_MODE bit = 0b, SDO/$\overline{DRDY}$ is the previous state until the first SCLK. Otherwise, SDO/$\overline{DRDY}$ follows $\overline{DRDY}$.
B. Data is two bytes (16-bit resolution) or three bytes (24-bit resolution)
C. In synchronized and start/stop modes, $\overline{DRDY}$ returns high at the 8th SCLK falling edge. In one-shot mode, $\overline{DRDY}$ remains low until a new conversion is started.

Figure 8-31. Conversion Data Read, Short Format

Figure 8-32 shows the long format of the read conversion data operation, which includes the STATUS header byte, three bytes of data, and the CRC byte. This example shows the option of full-duplex operation when a register command is input at the same time the conversion data is output. For the no-operation command, the ending input bytes are 00h, 00h, and D7h. The data output CRC (CRC-OUT) includes the STATUS byte and the conversion data bytes. If the conversion data readback is ended after the 8th SCLK of reading the MSB data but before all the data has been read, the $\overline{DRDY}$ pin goes high and the DRDY bit of the STATUS byte goes low to indicate data has been read.



A. Optional CRC byte. If CRC byte is disabled, the frame shortens by 1 byte
B. Optional STATUS header. If STATUS header byte is disabled, the frame shortens by 1 byte
C. Data is two bytes (16-bit resolution) or three bytes (24-bit resolution)
D. If the SDO_MODE bit = 0, previous state of SDO/$\overline{DRDY}$ until SCLK begins. Otherwise, SDO/$\overline{DRDY}$ follows $\overline{DRDY}$.

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E. In synchronized and start/stop modes, $\overline{DRDY}$ returns high at 16th SCLK falling edge (8th bit of the MS data byte). In one-shot mode, $\overline{DRDY}$ stays low until a new conversion is started.

Figure 8-32. Conversion Data Read, Long Format

Conversion data can be read asynchronous to $\overline{DRDY}$. When the conversion data is read close to the $\overline{DRDY}$ falling edge, there is uncertainty whether previous data or new data is output. If the shift operation starts at least one f_{MOD} before $\overline{DRDY}$ then old data is output. Similarly, if the shift operation starts at least one f_{MOD} after $\overline{DRDY}$, then new data is output. The DRDY bit of the STATUS header indicates if the data is old (previously read) or new.

8.5.6.1 Conversion Data Code

The conversion data is coded in two's-complement notation, MSB first (sign bit). Table 8-13 shows the output code for standard and extended input ranges for 24-bit resolution. The conversion code clips to positive and negative full-scale values when the input signal exceeds the positive and negative input range.

Table 8-13. 24-bit Two's-Complement Output Code

DIFFERENTIAL INPUT VOLTAGE (V) (1)	24-BIT OUTPUT CODE(2)	
	STANDARD RANGE	EXTENDED RANGE
$1.25 \cdot k \cdot V_{REF} \cdot (2^{23} - 1) / 2^{23}$	7FFFFFh	7FFFFFh
$k \cdot V_{REF} \cdot (2^{23} - 1) / 2^{23}$	7FFFFFh	666666h
$k \cdot V_{REF} / 2^{23}$	000001h	000001h
0	000000h	000000h
$-k \cdot V_{REF} / 2^{23}$	FFFFFFh	FFFFFFh
$-k \cdot V_{REF}$	800000h	99999Ah
$-1.25 \cdot k \cdot V_{REF}$	800000h	800000h

(1) k = 1 or 2, depending on 1x or 2x input range option.
(2) Ideal output code, excluding offset, gain, linearity and noise errors.

The ADC can be programmed to output 16-bit data. The data mode is selected by the DATA bit of register CONFIG4. The 16-bit data option limits SNR to 98.1 dB due to quantization noise.

8.5.6.2 Data Ready

There are several options to determine when conversion data are ready for readback.

1. Hardware: Monitor $\overline{DRDY}$ or SDO/$\overline{DRDY}$
2. Software: Monitor the DRDY bit of the STATUS header byte
3. Clock count: Count the number of ADC clocks to calculate the conversion time

8.5.6.2.1 Hardware Method

$\overline{DRDY}$ is driven low when conversion data are ready. $\overline{DRDY}$ is driven high at the 8th SCLK rising edge during readback of the conversion data most-significant byte (Synchronized and Start/Stop control modes only). $\overline{DRDY}$ also drives high when a conversion is restarted. If programmed to standby mode (STBY_MODE bit = 1b), $\overline{DRDY}$ is driven high three f_{CLK} cycles after it transitions low. $\overline{DRDY}$ is active whether $\overline{CS}$ is high or low. If conversion data are not read, $\overline{DRDY}$ pulses high just prior to the next falling edge. See the Conversion Control section for details of $\overline{DRDY}$ operation for each of the three conversion control modes.

To reduce the number of control lines across an isolation barrier, SDO/$\overline{DRDY}$ can be used in place of $\overline{DRDY}$ for data ready detection. $\overline{CS}$ must be low to sample the SDO/$\overline{DRDY}$ output pin. Figure 8-33 shows the operation of the $\overline{DRDY}$ and SDO/$\overline{DRDY}$ pins. If the SDO_MODE bit is programmed to 1b, SDO/$\overline{DRDY}$ is in dual-function mode. When $\overline{CS}$ is first taken low, SDO/$\overline{DRDY}$ mirrors the state of the $\overline{DRDY}$ pin. At the first rising edge of SCLK, SDO/$\overline{DRDY}$ changes to data output mode. When the data read operation is complete (24th falling edge of SCLK, 40th edge if CRC and STATUS header are included), SDO/$\overline{DRDY}$ changes back to the data ready mode, mirroring $\overline{DRDY}$.

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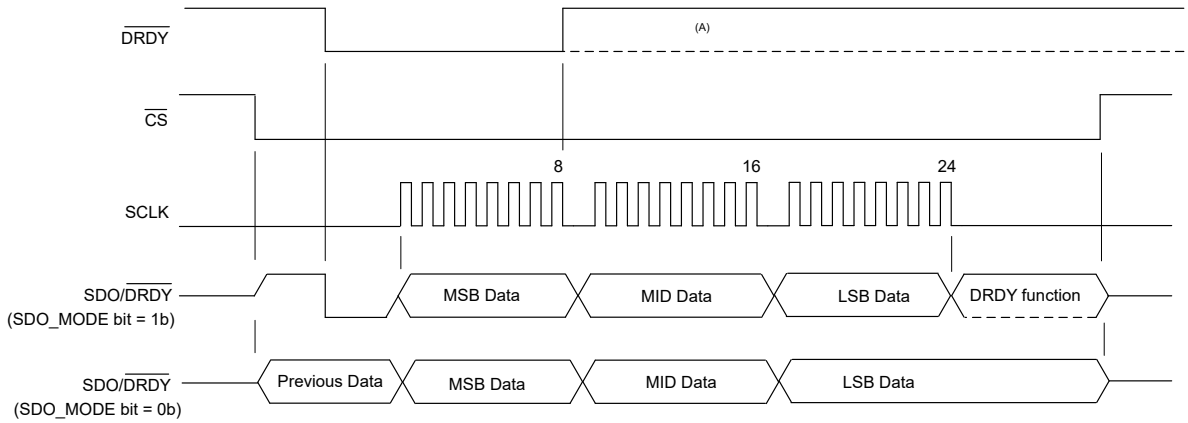

A. In synchronized and start/stop modes, $\overline{\text{DRDY}}$ returns high at the 8th SCLK falling edge (8th bit of MSB data). In one-shot mode, $\overline{\text{DRDY}}$ stays low until a new conversion is started.

Figure 8-33. $\overline{\text{DRDY}}$ and SDO/ $\overline{\text{DRDY}}$ Function

8.5.6.2.2 Software Method

The DRDY bit (bit 0 of STATUS header and STATUS register) indicates new data are ready. If DRDY = 1b, then the data are new since the last read operation, otherwise the previous conversion data is supplied. After the data are read, the bit remains at 0b until the next conversion data are ready. To avoid missing data, poll the bit by reading the STATUS header byte with the data at least as often as the period of f_{DATA}.

8.5.6.3 STATUS Header

A STATUS header can be prefixed to the conversion data. See Table 8-18 for the STATUS header field descriptions. The STATUS header is enabled by setting the STATUS bit of the CONFIG4 register. The STATUS header sent with the data is the same content as the STATUS register.

8.5.7 Daisy-Chain Connection

Daisy-chaining simplifies the SPI I/O line connections to a host controller for applications that use multiple ADCs. The daisy-chain connection links together one ADC SDO/$\overline{\text{DRDY}}$ output pin to another ADC SDI input pin so the linked devices appear as one expanded-register device to the host controller. There is no special programming for this mode, but instead, simply apply additional shift clocks to access all the ADCs in the chain. The output frame size of all devices must be the same and configured synchronously to all device in the chain (for example, during set up of 16-bit or 24-bit resolution, STATUS and CRC byte options).

Figure 8-34 shows four devices in a daisy-chain configuration. ADCS127L11 (1) connects SDI to MOSI of the host while ADS127L11 (4) connects SDO/$\overline{\text{DRDY}}$ to MISO of the host. The shift operation is simultaneous for all ADCs in the chain. When shifting data, the data on SDI passes through to SDO/$\overline{\text{DRDY}}$ to drive SDI of the next device in the chain. The shift operation continues until the last device in the chain is reached. The data frame ends when $\overline{\text{CS}}$ is taken high, at which time the input data residing in each device is interpreted. Due to the variable number of possible devices connected in a chain, $\overline{\text{CS}}$ is required to mark the end of the data frame. The SDO/$\overline{\text{DRDY}}$ pin must always be programmed to the data output-only mode.

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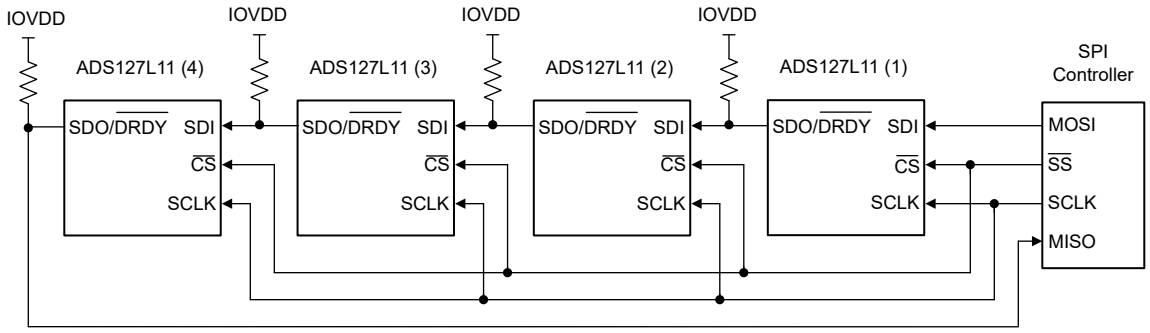
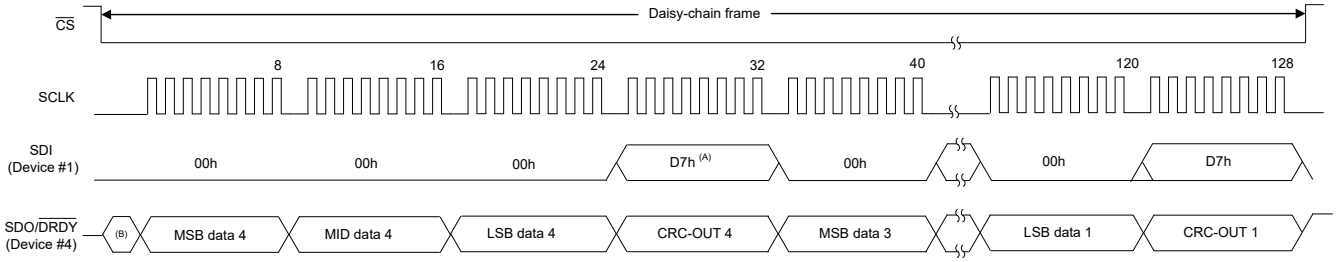


Figure 8-34. Daisy-Chain Connection

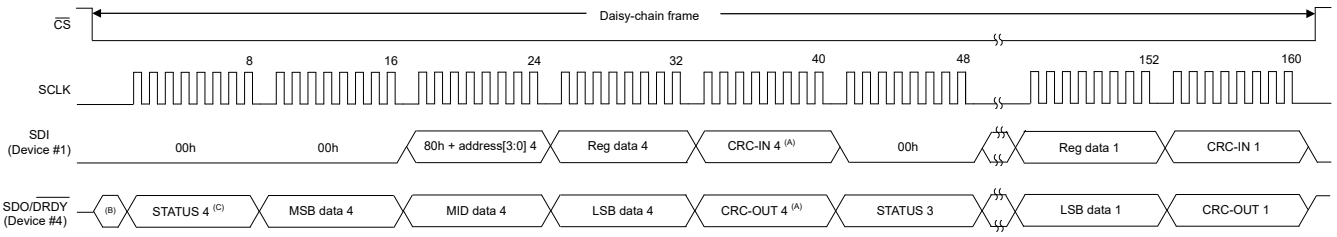
Figure 8-35 shows the clock sequence to read conversion data in daisy-chain mode of the connection shown in Figure 8-34. The example illustrates 24-bit data, SPI CRC mode enabled and the Status byte disabled (32-bit output frame). The conversion data of ADC (4) is the first data in the sequence, followed the data of ADC (3), and so on. The total number of clocks needed is given by the number of bits per frame times the number of devices. In this example, 32-bit output frames times 4 devices result in 128 total number of clocks. The input CRC value for the no operation command (00h, 00h) is D7h. Keep SDI low while reading conversion data to avoid clocking in 1023 consecutive 1s which will reset the device.



A. Optional CRC byte. If CRC mode is disabled, the frame shortens by 1 byte.
B. Previous state of SDO/$\overline{\text{DRDY}}$ before SCLK is applied.

Figure 8-35. Read Conversion Data in Daisy-Chain Mode

To input a command in daisy-chain mode, the host first shifts the input command intended for the last device in the chain. The input data of ADC (4) is first, followed by the input data of ADC (3), and so forth. To keep operation consistent, send the same command type to each device. Figure 8-36 shows the input data sequence for daisy-chain write register operation of Figure 8-34. The read register operation requires a second daisy-chain frame to shift out the actual register data.



A. Optional CRC byte. If CRC mode is disabled, the frame shortens by 1 byte.
B. Previous state of SDO/ $\overline{\text{DRDY}}$ before SCLK is applied.
C. Optional STATUS header. If STATUS header is disabled, the frame shortens by1 byte.

Figure 8-36. Write Register Data in Daisy-Chain Mode

Due to the constraints of SPI timing, the maximum SCLK frequency in daisy-chain mode is 16.5 MHz. The maximum number of devices connected in a chain is given by the data rate, the SCLK frequency and the number of bits per frame, as shown in Equation 8.

$$\text{Maximum devices in a chain} = \text{floor}[f_{SCLK}/(f_{DATA} \cdot \text{bits per frame})] \quad (8)$$

For example, if f_{SCLK} = 16.5 MHz, f_{DATA} = 100 kSPS, with a 40-bit frame, the maximum number of devices in a daisy-chain connection = floor[16.5 MHz / (100 kHz · 40)] = 4.

8.5.8 3-Wire SPI Mode

The ADC operates in 3-wire SPI mode by grounding $\overline{CS}$. If $\overline{CS}$ is low at power-on, 3-wire mode is engaged. 3-wire mode is reset to 4-wire mode by taking $\overline{CS}$ high at any time. 3-wire or 4-wire status is indicated by bit 7 (CS_MODE) of STATUS.

In 3-wire mode, the beginning and ending of the frame is no longer controlled by $\overline{CS}$ but by the number of bits per frame. The number of bits is counted by the ADC to mark the beginning and ending of a frame. The number of bits must always be controlled by the host to maintain synchronization to the ADC and must always match the size of the output frame. There is no required wait time between frames. The number of bits per output frame depends on the device configuration. The possible size combinations of the output frame are shown in Table 8-10.

8.5.8.1 3-Wire SPI Mode Reset

In 3-wire SPI mode, an unintended SCLK could cause frame misalignment between the ADC and the host, losing the ability to communicate with the ADC. SPI is resynchronized by applying the reset pattern shown in Figure 8-37. The reset pattern is a minimum 63 consecutive 1s followed by one 0 at the 64th SCLK. The SPI is synchronized starting at the 65th SCLK. Once SPI synchronization is re-established, the entire device can be reset through the SPI by applying the input pattern shown in Reset by SPI Input Pattern.

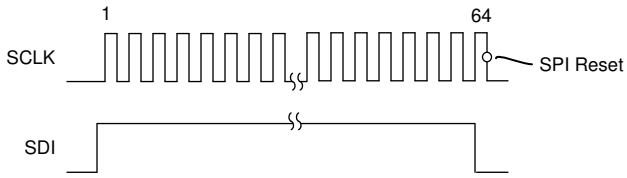


Figure 8-37. 3-Wire Mode SPI Reset Pattern

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8.6 Registers

Table 8-14 lists the register map of the ADS127L11. Register data are read/written one register at a time for each read/write operation. Writing to any register 4h through Eh results in conversion restart and loss of synchronization. If the ADC is idle (conversions stopped), new conversions are not started.

Table 8-14. ADS127L11 Register Map Overview

ADDRESS	REGISTER	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0h	DEV_ID	00h	DEV_ID[7:0]							
1h	REV_ID	xxh	REV_ID[7:0]							
2h	STATUS	xxh	CS_MODE	ALV_FLAG	POR_FLAG	SPI_ERR	REG_ERR	ADC_ERR	MOD_FLAG	DRDY
3h	CONTROL	00h	RESET[5:0]						START	STOP
4h	MUX	00h	RESERVED						MUX[1:0]	
5h	CONFIG1	00h	RESERVED	REF_RNG	INP_RNG	VCM	REFP_BUF	RESERVED	AINP_BUF	AINN_BUF
6h	CONFIG2	00h	EXT_RNG	RESERVED	SDO_MODE	START_MODE[1:0]		SPEED_MODE	STBY_MODE	PWDN
7h	CONFIG3	00h	DELAY[2:0]			FILTER[4:0]				
8h	CONFIG4	00h	CLK_SEL	CLK_DIV	OUT_DRV	RESERVED	DATA	SPI_CRC	REG_CRC	STATUS
9h	OFFSET	00h	OFFSET[23:16]							
Ah		00h	OFFSET[15:8]							
Bh		00h	OFFSET[7:0]							
Ch	GAIN	40h	GAIN[23:16]							
Dh		00h	GAIN[15:8]							
Eh		00h	GAIN[7:0]							
Fh	CRC	xxh	CRC[7:0]							

Table 8-15 lists the access codes of the registers.

Table 8-15. Register Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1 DEV_ID Register (Address = 0h) [reset = 00h]

DEV_ID is shown in Figure 8-38 and described in Table 8-16.

Return to the Register Map Overview.

Figure 8-38. DEV_ID Register

7	6	5	4	3	2	1	0
DEV_ID[7:0]							
R-00h							

Table 8-16. DEV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEV_ID[7:0]	R	00h	Device ID 00h = ADS127L11

8.6.2 REV_ID Register (Address = 1h) [reset = xxh]

REV_ID is shown in Figure 8-39 and described in Table 8-17.

Return to the Register Map Overview.

Figure 8-39. REV_ID Register

7	6	5	4	3	2	1	0
REVID[7:0]							
R-xxxxxxxxb							

Table 8-17. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REV_ID[7:0]	R	xxxxxxxxb	Die Revision ID (Die revision ID can change without notice)

8.6.3 STATUS Register (Address = 2h) [reset = xxh]

STATUS is shown in Figure 8-40 and described in Table 8-18.

Return to the Register Map Overview.

Figure 8-40. STATUS Register

7	6	5	4	3	2	1	0
CS_MODE	ALV_FLAG	POR_FLAG	SPI_ERR	REG_ERR	ADC_ERR	MOD_FLAG	DRDY
R-xb	R/W-xb	R/W-xb	R/W-0b	R/W-0b	R-0b	R-xb	R-0b

Table 8-18. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CS_MODE	R	xb	$\overline{CS}$ mode This bit indicates the selection of 4-wire or 3-wire SPI operation that is determined by the state of $\overline{CS}$ at power-on. 0b = 4-wire SPI operation ($\overline{CS}$ input is active) 1b = 3-wire SPI operation ($\overline{CS}$ tied low)
6	ALV_FLAG	R/W	xb	Analog Supply Low Voltage Flag This bit is set when a low voltage condition is detected on the analog power supplies. Write 1b to clear the flag to detect the next low voltage condition. 0b = No analog supply low-voltage since flag cleared 1b = Analog supply low-voltage detected
5	POR_FLAG	R/W	xb	Power-on reset (POR) Flag This bit indicates device reset at power-on or brown-out of the IOVDD supply or CAPD bypass output, or by a user-initiated reset. Write 1b to clear the flag to detect the next reset. 0b = No reset since flag cleared 1b = Device reset occurred

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Table 8-18. STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SPI_ERR	R/W	0b	SPI Communication CRC Error This bit assets when an SPI CRC input error is detected. When set, further register write operations are blocked, except to the STATUS register that allows clearing the SPI error (write 1b to clear the error). Register read operations remain functional. The SPI CRC error detection is enabled by the SPI_CRC bit (CONFIG4 register). 0b = No error 1b = SPI CRC error
3	REG_ERR	R/W	0b	Register Map CRC Error REG_ERR asserts when the programmed register map CRC (0Fh) value does not match the ADC calculated value. Write 1b to clear the register map CRC error. Set the REG_CRC bit (CONFIG4 register) to enable the register map error check. 0b = No error 1b = Register map CRC error
2	ADC_ERR	R	0b	Internal ADC Error ADC_ERR asserts when an internal error is detected. Reset the device. 0b = No ADC error 1b = ADC error detected
1	MOD_FLAG	R	xb	Modulator Overload Flag This bit sets if the input signal has exceeded the input range during a conversion cycle. The flag auto-resets at the beginning of the next conversion. 0b = No modulator overload detected 1b = Modulator overload detected
0	DRDY	R	0b	Data Ready Bit DRDY indicates new conversion data. The DRDY bit is the inversion of the $\overline{\text{DRDY}}$ pin. If desired, poll the bit to determine if conversion data is new or repeated since the previous read operation. DRDY = 0 indicates data was previously read. In one-shot mode, the bit remains at 1b until a new conversion is started. 0b = Data is not new (repeated data) 1b = Data is new (new conversion data, not for one-shot mode)

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8.6.4 CONTROL Register (Address = 3h) [reset = 00h]

CONTROL is shown in Figure 8-41 and described in Table 8-19.

Return to the Register Map Overview.

Figure 8-41. CONTROL Register

7	6	5	4	3	2	1	0
RESET[5:0]						START	STOP
W-000000b						W-0b	W-0b

Table 8-19. CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESET[5:0]	W	000000b	Device Reset Write 010110b to reset the ADC. The adjacent START and STOP bits must also be written with 0b values to reset the ADC. Always reads 0.
1	START	W	0b	Start Conversion Conversions are started/re-started by writing 1b. In one-shot mode, one conversion is started. In start/stop mode, conversions continue until stopped by the STOP bit. This bit has no effect in the synchronized mode. Writing 1b to both START and STOP bits has no effect. Always reads 0. 0b = No operation 1b = Start or re-start conversion
0	STOP	W	0b	Stop Conversion This bit stops conversions. The current conversion will run to completion. This bit has no effect in the synchronized mode. Writing 1b to both START and STOP at the same time has no effect. Always reads 0. 0b = No operation 1b = Stop conversion after the current conversion completes

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8.6.5 MUX Register (Address = 4h) [reset = 00h]

MUX is shown in Figure 8-42 and described in Table 8-20.

Return to the Register Map Overview.

Figure 8-42. MUX Register

7	6	5	4	3	2	1	0
RESERVED						MUX[1:0]	
R-000000b						R/W-00b	

Table 8-20. MUX Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	000000b	
1:0	MUX[1:0]	R/W	00b	Input Channel Selection These bits select the input polarity 00b = Normal polarity 01b = Inverted polarity 10b = Offset test: AINP and AINN disconnected, ADC inputs internally shorted to (AVDD1 + AVSS)/2 11b = Common-mode test: ADC inputs internally shorted and connected to AINP

8.6.6 CONFIG1 Register (Address = 5h) [reset = 00h]

CONFIG1 is shown in Figure 8-43 and described in Table 8-21.

Return to the Register Map Overview.

Figure 8-43. CONFIG1 Register

7	6	5	4	3	2	1	0
RESERVED	REF_RNG	INP_RNG	VCM	REFP_BUF	RESERVED	AINP_BUF	AINN_BUF
R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-21. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	
6	REF_RNG	R/W	0b	Voltage Reference Range Selection This bit selects the low or high reference operating range. In the high-voltage reference range, the input range selection is overridden to 1x. 0b = Low reference range 1b = High reference range
5	INP_RNG	R/W	0b	Input Range Selection This bit selects the 1x or 2x input range. See the Input Range section for more details. 0b = 1x input range 1b = 2x input range
4	VCM	R/W	0b	VCM Output Enable This bit enables the (AVDD1 + AVSS)/2 output voltage to the VCM pin. 0b = Disabled 1b = Enabled
3	REFP_BUF	R/W	0b	Reference Positive Buffer Enable This bit enables the positive reference input precharge buffer. 0b = Disabled 1b = Enabled
2	RESERVED	R/W	0b	
1	AINP_BUF	R/W	0b	Analog Input Positive Buffer Enable This bit enables the positive analog input precharge buffer. 0b = Disabled 1b = Enabled
0	AINN_BUF	R/W	0b	Analog Input Negative Buffer Enable This bit enables the negative input precharge buffer. 0b = Disabled 1b = Enabled

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8.6.7 CONFIG2 Register (Address = 6h) [reset = 00h]

CONFIG2 is shown in Figure 8-44 and described in Table 8-22.

Return to the Register Map Overview.

Figure 8-44. CONFIG2 Register

7	6	5	4	3	2	1	0
EXT_RNG	RESERVED	SDO_MODE	START_MODE[1:0]		SPEED_MODE	STBY_MODE	PWDN
R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-0b

Table 8-22. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EXT_RNG	R/W	0b	Extended Input Range Enable. This bit extends the standard input range by 25%. See the Input Range section for more details. 0b = Standard input range 1b = Input range extended 25%
6	RESERVED	R/W	0b	
5	SDO_MODE	R/W	0b	SDO/$\overline{\text{DRDY}}$ Mode Selection This bit programs the mode of the SDO/$\overline{\text{DRDY}}$ pin. For daisy-chain connection of ADCs, use the data-output only mode. See the Serial Data Output/Data Ready (SDO/$\overline{\text{DRDY}}$) section for more details. 0b = Data-output only mode 1b = Dual mode: data output and data ready
4:3	START_MODE[1:0]	R/W	0b	START Mode These bits program the mode of the START pin and also the functionality of the START/STOP register control bits. See the Conversion Control section for more details. 00b = Start/Stop mode 01b = One-shot mode 10b = Synchronized mode 11b = Reserved
2	SPEED_MODE	R/W	0b	Speed Mode Selection This bit programs the speed mode of the device. The input clock frequency corresponds to the mode. 0b = High-speed mode (standard f_{CLK} = 25.6 MHz) 1b = Low-speed mode (standard f_{CLK} = 3.2 MHz)
1	STBY_MODE	R/W	0b	Standby Mode Selection This bit enables the low-power Standby mode after conversions are stopped. 0b = Idle mode; ADC remains fully powered when conversions are stopped 1b = Standby mode; ADC is powered down when conversions are stopped

ADVANCE INFORMATION

Table 8-22. CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PWDN	R/W	0b	Software Power Down Enable This bit powers down the ADC. All functions are powered-off except for SPI operation and the digital LDO to retain user register settings. 0b = Disabled 1b = Enabled

8.6.8 CONFIG3 Register (Address = 7h) [reset = 00h]

CONFIG3 is shown in Figure 8-45 and described in Table 8-23.

Return to the Register Map Overview.

Figure 8-45. CONFIG3 Register

7	6	5	4	3	2	1	0
DELAY[2:0]			FILTER[4:0]				
R/W-000b			R/W-00000b				

Table 8-23. CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DELAY[2:0]	R/W	000b	Conversion-Start Delay Time Selection Program a delay time from the input of START to the actual start of the *first* conversion. Delay time is given in number of f_{MOD} clock cycles ($f_{MOD} = f_{CLK} / 2$). 000b = 0 001b = 4 010b = 8 011b = 16 100b = 32 101b = 128 110b = 512 111b = 1024

ADVANCE INFORMATION

Table 8-23. CONFIG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	FILTER[4:0]	R/W	00000b	Digital Filter Mode and Oversampling Ratio Selection Configure the digital filter. The digital filter has five modes: wideband, sinc4, sinc4 + sinc1, sinc3, and sinc3 + sinc1, each with selectable value of OSR. 00000 = wideband, OSR = 32 00001 = wideband, OSR = 64 00010 = wideband, OSR = 128 00011 = wideband, OSR = 256 00100 = wideband, OSR = 512 00101 = wideband, OSR = 1024 00110 = wideband, OSR = 2048 00111 = wideband, OSR = 4096 01000 = sinc4, OSR = 12 01001 = sinc4, OSR = 16 01010 = sinc4, OSR = 24 01011 = sinc4, OSR = 32 01100 = sinc4, OSR = 64 01101 = sinc4, OSR = 128 01110 = sinc4, OSR = 256 01111 = sinc4, OSR = 512 10000 = sinc4, OSR = 1024 10001 = sinc4, OSR = 2048 10010 = sinc4, OSR = 4096 10011 = sinc4, OSR = 32 + sinc1, OSR = 2 10100 = sinc4, OSR = 32 + sinc1, OSR = 4 10101 = sinc4, OSR = 32 + sinc1, OSR = 10 10110 = sinc4, OSR = 32 + sinc1, OSR = 20 10111 = sinc4, OSR = 32 + sinc1, OSR = 40 11000 = sinc4, OSR = 32 + sinc1, OSR = 100 11001 = sinc4, OSR = 32 + sinc1, OSR = 200 11010 = sinc4, OSR = 32 + sinc1, OSR = 400 11011 = sinc4, OSR = 32 + sinc1, OSR = 1000 11100 = sinc3, OSR = 26667 11101 = sinc3, OSR = 32000 11110 = sinc3, OSR = 32000 + sinc1, OSR = 3 11111 = sinc3, OSR = 32000 + sinc1, OSR = 5

ADVANCE INFORMATION

8.6.9 CONFIG4 Register (Address = 8h) [reset = 00h]

CONFIG4 is shown in Figure 8-46 and described in Table 8-24.

Return to the Register Map Overview.

Figure 8-46. CONFIG4 Register

7	6	5	4	3	2	1	0
CLK_SEL	CLK_DIV	OUT_DRV	RESERVED	DATA	SPI_CRC	REG_CRC	STATUS
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-24. CONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLK_SEL	R/W	0b	Clock Selection Select internal or external clock operation. 0b = Internal clock operation 1b = External clock operation
6	CLK_DIV	R/W	0b	External Clock Division Selection This bit is used to divide the external clock by 1/8. 0b = External clock division by 1 1b = External clock division by 8
5	OUT_DRV	R/W	0b	Digital Output Drive Selection Select the drive strength of the digital outputs. 0b = Full drive strength 1b = ½ drive strength
4	RESERVED	R	0b	
3	DATA	R/W	0b	Data Resolution Selection This bit selects the conversion data resolution 0b = 24-bit resolution 1b = 16-bit resolution
2	SPI_CRC	R/W	0b	SPI CRC Enable This bit enables SPI CRC error checking. The device verifies the input CRC while appending an output CRC to the output data. The SPI_ERR bit of the STATUS byte is set if a CRC error is detected. Write 1b to the SPI_ERR bit to clear the error. 0b = SPI CRC function disabled 1b = SPI CRC function enabled
1	REG_CRC	R/W	0b	Register Map CRC Enable This bit enables the register map CRC error check. The user writes the CRC value to register 0Fh, calculated over registers 0h,1h and 4h to Eh. An internally calculated CRC value is compared to the written register value. The REG_ERR bit of the STATUS byte is set if the CRC values do not match. 0b = Register map CRC function disabled 1b = Register map CRC function enabled

Table 8-24. CONFIG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	STATUS	R/W	0b	STATUS Byte Output Enable Program this bit to prefix the STATUS byte to the conversion data output. 0b = Status byte not prefixed to the conversion data 1b = Status byte prefixed to the conversion data

8.6.10 OFFSET Registers (Addresses = 9h, Ah, Bh) [reset = 00h, 00h, 00h]

OFFSET registers are shown in Figure 8-47 and described in Table 8-25.

Return to the Register Map Overview.

Figure 8-47. OFFSET Registers

7	6	5	4	3	2	1	0
OFFSET[23:16]							
R/W-00000000b							
7	6	5	4	3	2	1	0
OFFSET[15:8]							
R/W-00000000b							
7	6	5	4	3	2	1	0
OFFSET[7:0]							
R/W-00000000b							

Table 8-25. OFFSET Registers Field Description

Bit	Field	Type	Reset	Description
23:0	OFFSET[23:0]	R/W	000000h	User Offset Calibration Value Three registers form the 24-bit offset calibration word. OFFSET[23:0] is in two's-complement representation and is subtracted from the conversion result. The offset operation precedes the gain operation.

ADVANCE INFORMATION

8.6.11 Gain Registers (Addresses = Ch, Dh, Eh) [reset = 40h, 00h, 00h]

GAIN registers are shown in Figure 8-48 and described in Table 8-26.

Return to the Register Map Overview.

Figure 8-48. GAIN Registers

7	6	5	4	3	2	1	0
GAIN[23:16]							
R/W-01000000b							
7	6	5	4	3	2	1	0
GAIN[15:8]							
R/W-00000000b							
7	6	5	4	3	2	1	0
GAIN[7:0]							
R/W-00000000b							

Table 8-26. GAIN Registers Field Description

Bit	Field	Type	Reset	Description
23:0	GAIN[23:0]	R/W	400000h	User Gain Calibration Value Three registers form the 24-bit gain calibration word. GAIN[23:0] is in straight-binary representation and is normalized at 400000h to equal gain of 1. The conversion data is multiplied by GAIN[23:0] / 400000h after the offset operation.

8.6.12 CRC Register (Address = Fh) [reset = xxh]

CRC is shown in Figure 8-49 and described in Table 8-27.

Return to the Register Map Overview.

Figure 8-49. CRC Register

7	6	5	4	3	2	1	0
CRC[7:0]							
R/W-xxxxxxxxb							

Table 8-27. CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CRC[7:0]	R/W	xxh	Register Map CRC Value. The register map CRC value is written by the user, calculated over registers 0h,1h and 4h through Eh. The CRC value is compared to an internally calculated value. If the values do not match, the REG_ERR bit is set in the STATUS header and STATUS register. The register CRC check is enabled by the REG_CRC bit.

8.6.13 Register Map CRC

The register map CRC option is used to detect unintended changes to the register map values. The user writes the register map CRC value to the CRC register as basis for detection. The CRC is calculated over registers 00h to 0Eh, skipping registers 02h and 03h (STATUS and CONTROL registers). The user-written CRC value is continuously checked against an internally calculated value. If the values do not match, the REG_ERR bit in STATUS register sets. If set, correct the register and CRC values then write 1b to clear the REG_ERR flag. No other action is taken by the ADC in the event of a detected error. The register map CRC check is enabled/disabled by the REG_CRC bit of the CONFIG4 register.

Be sure to read the REV_ID register of the individual ADC when calculating the CRC because the REV_ID can change in production without notice. Set the REG_CRC bit to 1 (enable) when calculating the CRC. The CRC is the 8-bit remainder of the bitwise exclusive-OR (XOR) operation of the variable length argument by the CRC polynomial. The CRC is based on the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X^1 + 1$. The nine coefficients of the polynomial are: 100000111. The CRC calculation is preset to all 1s, same as used for the SPI CRC calculation.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The high-performance capability of the ADS127L11 is achievable once familiar with the requirements of the input driver, anti-alias filter, reference voltage, SPI clocking and PCB layout. The following sections provide the design guidelines.

9.1.1 SPI Operation

Although the ADC provides flexible clock options for the SPI interface and the range of IOVDD voltage, the following guidelines are recommended to achieve full data sheet performance.

1. Use SCLK that is phase coherent to CLK; ratios of 2:1, 1:1, 1:2, 1:4, and so on.
2. Minimize phase skew between SCLK and CLK (< 5 ns).
3. Operate IOVDD at the lowest voltage possible to reduce digital noise.
4. If IOVDD ≥ 3.3 V consider operating SCLK continuously over the full conversion period to spread noise over the full conversion period.
5. Keep the trace capacitance of SDO/$\overline{\text{DRDY}}$ ≤ 20 pF to reduce the peak currents associated with digital output transitions.

9.1.2 Input Driver

Choose a 10-MHz or greater gain-bandwidth driver for proper anti-alias filter attenuation at f_{MOD}. The ADC incorporates input precharge buffers that reduce the driver settling time requirement. If a 10-MHz or less gain-bandwidth driver is used, it is recommended to activate the input precharge buffers. For higher gain-bandwidth drivers, THD performance is incrementally improved with the use the input precharge buffers. For low speed mode operation, the modulator is sampling 1/8th slower (1.6 MHz) so the user has the option of disabling input precharge buffers to reduce power consumption.

9.1.3 Anti-Alias Filter

Input signals occurring near f_{MOD} (12.8 MHz in high-speed mode; 1.6 MHz in low-speed mode) foldback (or alias) to the passband resulting in data errors if the input signal is not low-pass filtered. The aliased frequency errors cannot be removed by post processing the data. The order of the anti-alias filter is heavily dependent on the selected OSR and the targeted signal attenuation at f_{MOD}. The larger the value of OSR - larger frequency ratio between f_{DATA} and f_{MOD} - the more relaxed the filter requirements are. For example, for OSR = 128 more than two decades of frequency separates f_{DATA} and f_{MOD}. With a filter corner frequency at f_{DATA}, a 3rd-order filter with 60-dB/decade attenuation provides greater than 120-dB alias rejection.

9.1.4 Reference Voltage

Use a reference voltage with low output noise and sufficient output drive strength for the sampled reference input. The ADC incorporates an optional reference precharge buffer for the positive branch that reduces the reference drive requirement. Because the modulator continuously samples the reference input whether conversions are active or inactive (except for Standby mode), the reference load remains constant. A 22-uF decoupling capacitor at the reference output and 1-µF + 0.1-µF capacitors across the reference input pins is sufficient to filter the sampled input.

ADVANCE INFORMATION

9.2 Typical Application

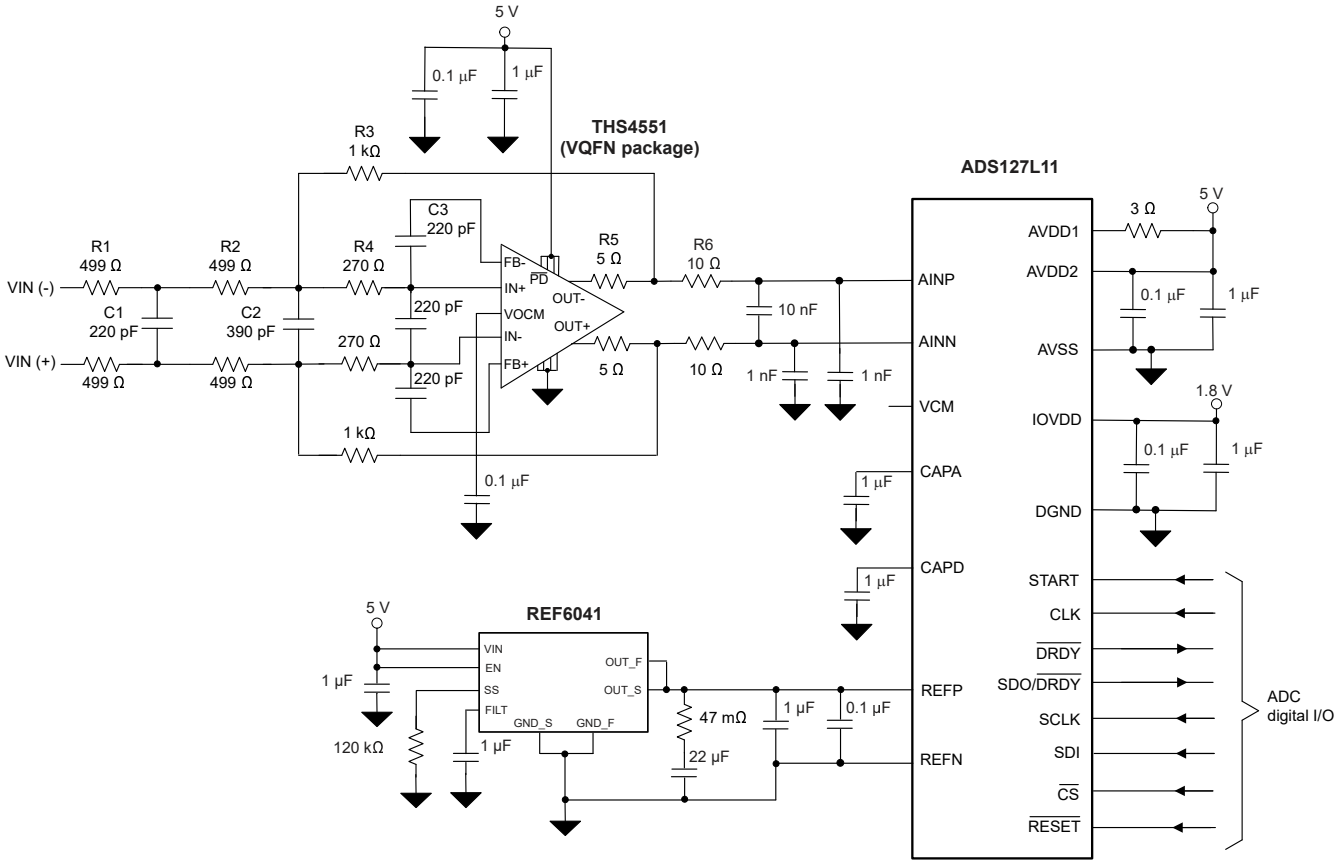


Figure 9-1. ADS127L11 Circuit Diagram

9.2.1 Design Requirements

Figure 9-1 shows an application circuit diagram of the ADS127L11. The goal of this application is to design an analog anti-alias filter for the ADC input to attenuate out-of-band signals at the modulator sample rate (f_{MOD}). The filter reduces passband fold-back (aliasing) errors of these frequencies. The requirement of the anti-alias filter is to provide 95-dB signal attenuation at the critical modulator-aliasing frequency (12.8 MHz in high-speed mode operation). It is also desired to maintain flat amplitude response and low phase error within the passband of the ADC.

Table 9-1 shows the design target values and the actual output values produced by the filter design.

Table 9-1. Anti-Alias Filter Design Requirements

PARAMETER	TARGET VALUE	ACTUAL VALUE
DC voltage gain	0 dB	0 dB
Attenuation at 12.8 MHz	95 dB	95 dB
–0.1-dB passband	200 kHz	240 kHz
–3-dB passband	500 kHz	500 kHz
Passband peaking	10 mdB	10 mdB
Filter phase shift at 200 kHz	–60°	–49°

9.2.2 Detailed Design Procedure

The anti-aliasing filter consists of a passive 1st-order input filter, an active 2nd-order filter, and a 1st-order output filter. The filter response is 4th-order overall. For this example, the filter performance satisfies the worst-case value of wideband-mode OSR (32), which results in less than two decades of frequency between Nyquist and f_{MOD} frequencies. This filter must provide the required attenuation in less than two decades of frequency. The filter roll-off is designed to begin just after the Nyquist frequency while providing 95 dB rejection at f_{MOD}. The total filter attenuation at f_{MOD} is the key function of the filter.

The THS4551 amplifier is selected because of the 150-MHz gain-bandwidth product (GBP) and 50-ns settling time. The amplifier's GBP is sufficient to maintain the filter's frequency response to 12.8 MHz, even with the dc-gain set to 15 dB. For example, applications where amplifier gain is used, a 10-MHz amplifier would have marginal GBP to adequately support the filter roll-off at the f_{MOD} frequency. The settling time of the THS4551 is suitable for driving the ADC's sampled inputs.

The design of the active section of the filter begins with an equal-R assumption (4x 1 kΩ) to establish the dc-gain. The dc-gain of the filter is $R_3/(R_1 + R_2)$. The choice of 1-kΩ resistors is a compromise of signal power dissipation of the resistors versus resistor thermal noise. The resistor thermal noise is approximately ½ the noise of the ADC.

The amplifier input resistor is divided into two 499-Ω resistors (R_1 and R_2) to implement the 1st-order filter with C_1. The 1st-order filter is decoupled from the 2nd-order active filter, but shares R_1 and R_2 to determine the corner frequency. The corner frequency is given by C_1 and the Thevenin resistance at each terminal of C_1 (R_{TH} = 2x 250 Ω).

Given an arbitrary selection of R_4 (2x 270 Ω in this case), the values of the 2x 220 pF (C3) feedback capacitors and the single 390 pF differential capacitor (C2) are determined by the filter design equations for the target values of filter f_O and filter Q. See the *Design Methodology for MFB Filters in ADC Interface Applications* application note for the filter design equations of the multiple-feedback active filter. The single 220-pF differential capacitor at the amplifier input is not a direct part the filter design but instead compensates for amplifier peaking. The 5-Ω resistors (R_5) isolate the amplifier outputs from stray capacitance.

The RC filter at the ADC inputs serves two functions. First, the filter adds a fourth pole to the overall filter response, thereby increasing the overall filter roll-off. The other function of the RC filter is a charge reservoir to filter the sampled input of the ADC. The charge reservoir reduces the instantaneous charge demand from the amplifier, maintaining low distortion and low gain error that otherwise can degrade due to incomplete amplifier settling. The values of the input filter are 2 x 10 Ω and 10 nF. The 10-Ω resistors are outside the THS4551 filter loop to isolate the amplifier outputs from the 10-nF capacitor to maintain stability.

Low voltage-coefficient C0G capacitors are used everywhere for the low distortion property. The amplifier gain resistors are 0.1% tolerance to maintain full THD performance. The ADC VCM output connection to the amplifier VOCM input pin is optional because the same function is provided by the amplifier.

See the *THS4551 Data Sheet* for additional examples of active filter design and application.

9.2.3 Application Curves

Figure 9-2 shows the amplitude response of the anti-alias filter alone, and the combined response of the ADC and anti-alias filter. As seen in the figure, the amplitude response of the filter is –95 dB at the first aliasing frequency at 12.8 MHz. Figure 9-3 shows the phase response of the anti-alias filter. The phase of the anti-alias filter at the 200-kHz Nyquist frequency is –49°.

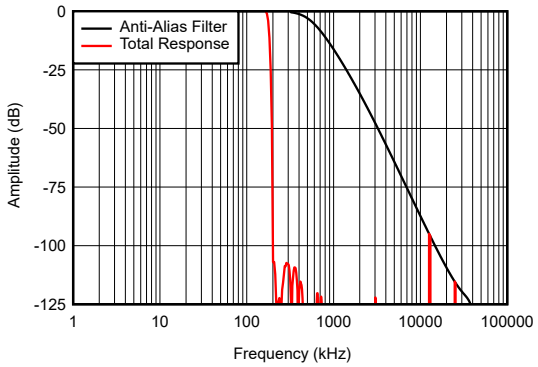


Figure 9-2. Amplitude Response vs Frequency with Anti-Alias Filter

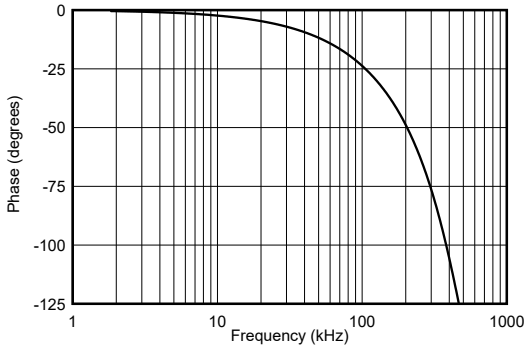


Figure 9-3. Phase Response vs Frequency of Anti-Alias Filter

ADVANCE INFORMATION

10 Power Supply Recommendations

The ADC has three analog power supplies and one digital power supply. Power supplies AVDD1 and AVSS establish the type of input range, either bipolar or unipolar. Bipolar input signals are permissible when bipolar supplies are used for AVDD1 and AVSS. If using a single power supply for AVDD1 (with AVSS connected to DGND), only unipolar input signals are possible.

AVDD2 powers the ADC modulator. The AVDD2 supply voltage is with respect to AVSS. IOVDD is the digital power supply with respect to DGND.

The specified voltage range for the power supplies is given in the Recommended Operating Conditions . For a minimum power supply configuration, a single 5-V supply can be used for AVDD1, AVDD2 and IOVDD, with AVSS connected to ground. IOVDD should always have separate bypass capacitors to DGND.

Proper supply bypassing is essential to achieve data sheet performance. The ADC requires additional capacitors for the CAPA and CAPD pins and bypass capacitors for the reference input pins. Place the capacitors close to the device pins using short, direct traces with the smaller capacitor value placed closest to the device pins.

The following are the recommended external capacitors and resistors for the ADC pins.

1. AVDD1 to AVSS
   a. Parallel combination of 1-µF and 0.1-µF capacitors placed between the pins
   b. 3-Ω resistor placed in-series between the bypass capacitors and the AVDD1 pin
2. AVDD2 to AVSS: parallel combination of 1-µF and 0.1-µF capacitors placed between the pins
3. IOVDD to DGND: parallel combination of 1-µF and 0.1-µF capacitors placed between the pins
4. CAPA to AVSS: 1-µF capacitor placed between the pins
5. CAPD to DGND: 1-µF capacitor placed between the pins
6. REFP to REFN: parallel combination of 1-µF and 0.1-µF capacitors placed between the pins

The layout example of Figure 11-1 illustrates placement of the components.

The power supplies do not require special sequencing and can be powered up in any order, but in no case must any analog or digital input exceed the respective AVDD1 and AVSS (analog) or IOVDD (digital) power-supply voltages. An internal reset is performed after the IOVDD power supply voltage is applied.

The ADC is ready for operation at power-up when the $\overline{\text{DRDY}}$ pin transitions high. If START is high, the ADC begins the first conversion, resulting in $\overline{\text{DRDY}}$ transitioning low 170 µs later.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

To achieve data sheet performance, use a minimum four-layer PCB board with the inner layers dedicated to ground and power planes. Best performance is achieved by combining the analog and digital grounds on a single, unbroken ground plane. In some layout geometries however, it may be necessary to use separate analog and digital grounds to help direct digital currents away from the analog ground (such as pulsing LED indicators, relays, and so on). In this case, consider separate ground return paths for these loads. When separate analog and digital grounds are used, join the grounds at the ADC.

The power plane layer is used to route the power supplies to the ADC.

The top and bottom layers route the analog and digital signals. Route the input signal as a matched differential pair throughout the signal chain to reduce differential noise coupling. Avoid crossing or adjacent placement of digital signals with the analog signals. This is especially true for high-frequency digital signals such as the clock input, and SPI signals, SCLK and SDO/$\overline{\text{DRDY}}$. The pin placement of both ADC package options minimizes the need to cross digital and analog signals.

Place the voltage reference close to the ADC. Orient the reference such that the reference ground pin is close to the ADC REFN pin. Place the reference input bypass capacitors directly at the ADC pins. Use reference bypass capacitors for each ADC in multi-channel systems. In this case, connect the reference ground pin to the ground plane (or to AVSS in bipolar supply systems) at one point and route REFP and REFN as paired-traces to each ADC.

11.2 Layout Example

Figure 11-1 is a layout example of the circuit diagram shown in Figure 9-1, with the ADC shown in the QFN package option. A four-layer PCB is used, with the inner layers dedicated as ground and power planes. Cutouts are used on the plane layers under the amplifier input pins to reduce stray capacitance. Thermal vias under the ADS127L11 are not used to allow placement of the CAPA bypass capacitor on the bottom layer. Place the smaller of the parallel supply bypass capacitors closest to the device supply pins.

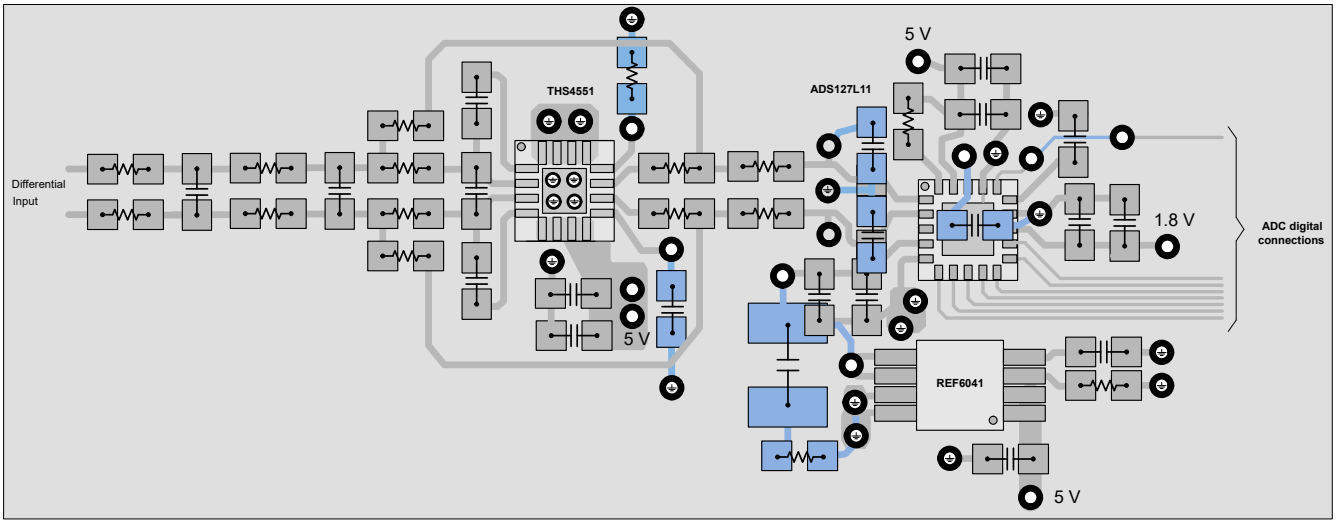


Figure 11-1. Layout Example of Typical Application Circuit

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *THS4551 Low-Noise, Precision, 150-MHz, Fully Differential Amplifier* data sheet
- Texas Instruments, *REF60xx High-Precision Voltage Reference With Integrated ADC Drive Buffer* data sheet
- Texas Instruments, *IEPE Vibration Sensor Interface Reference Design for PLC Analog Input* TI design

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

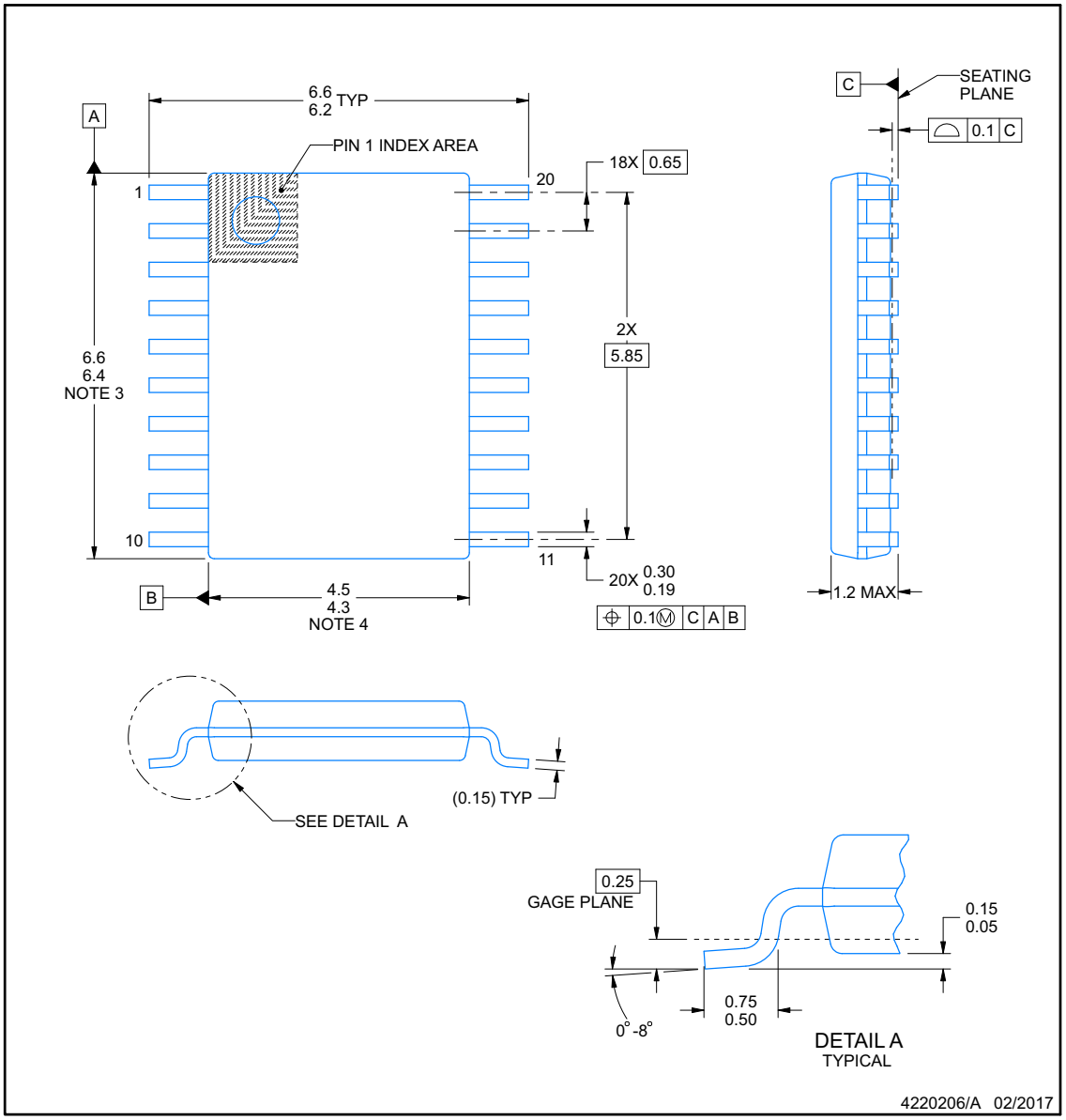
ADVANCE INFORMATION

13.1 Mechanical Data

PACKAGE OUTLINE

PW0020A — **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

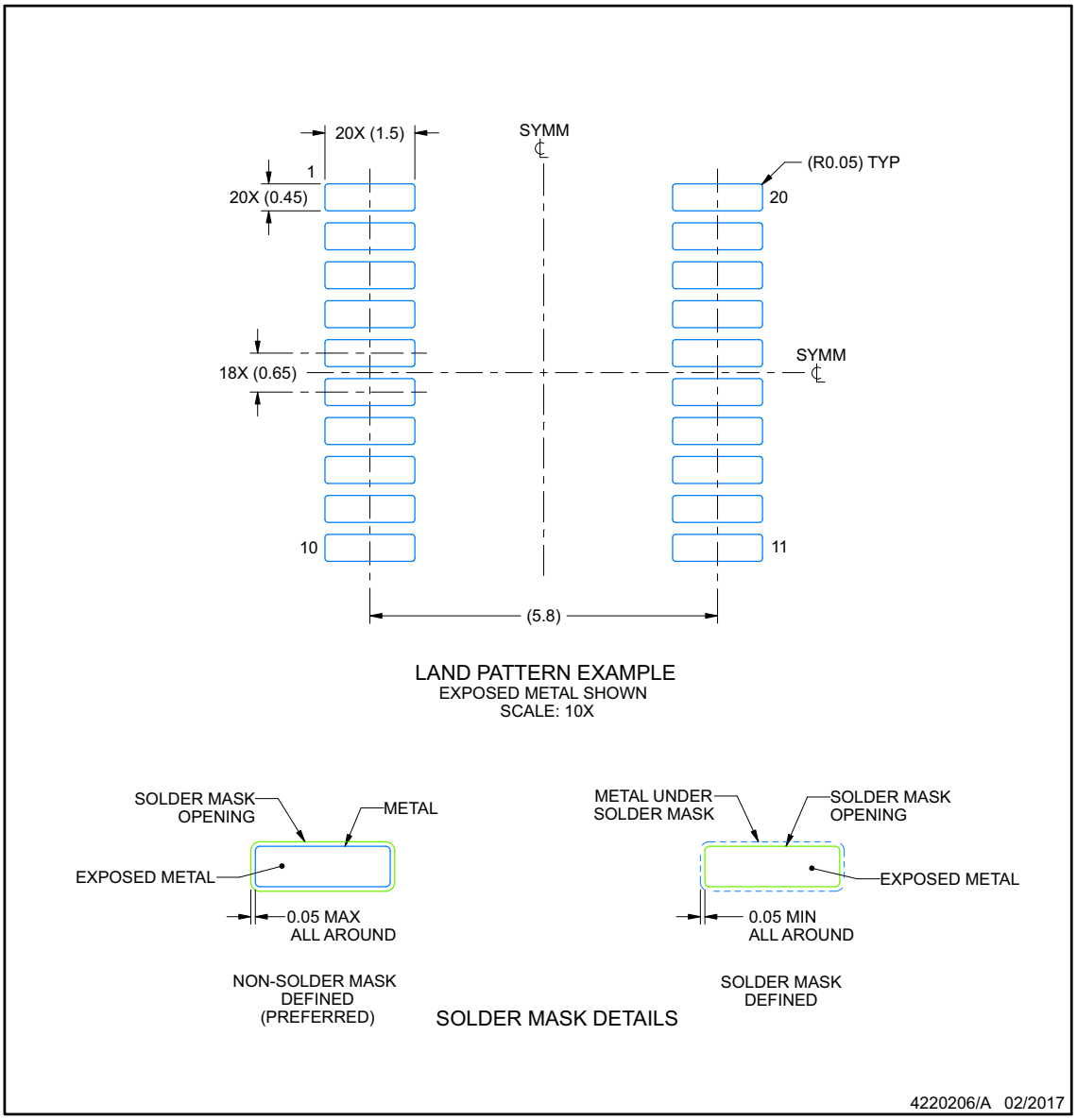
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

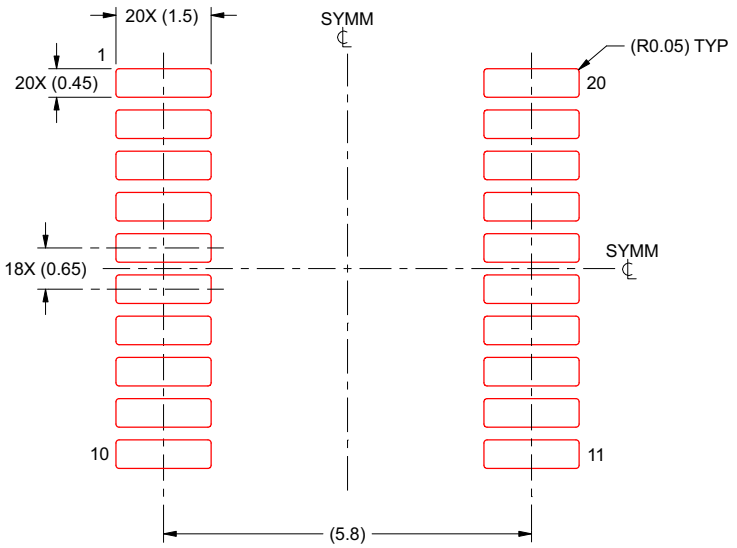
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PW0020A — **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

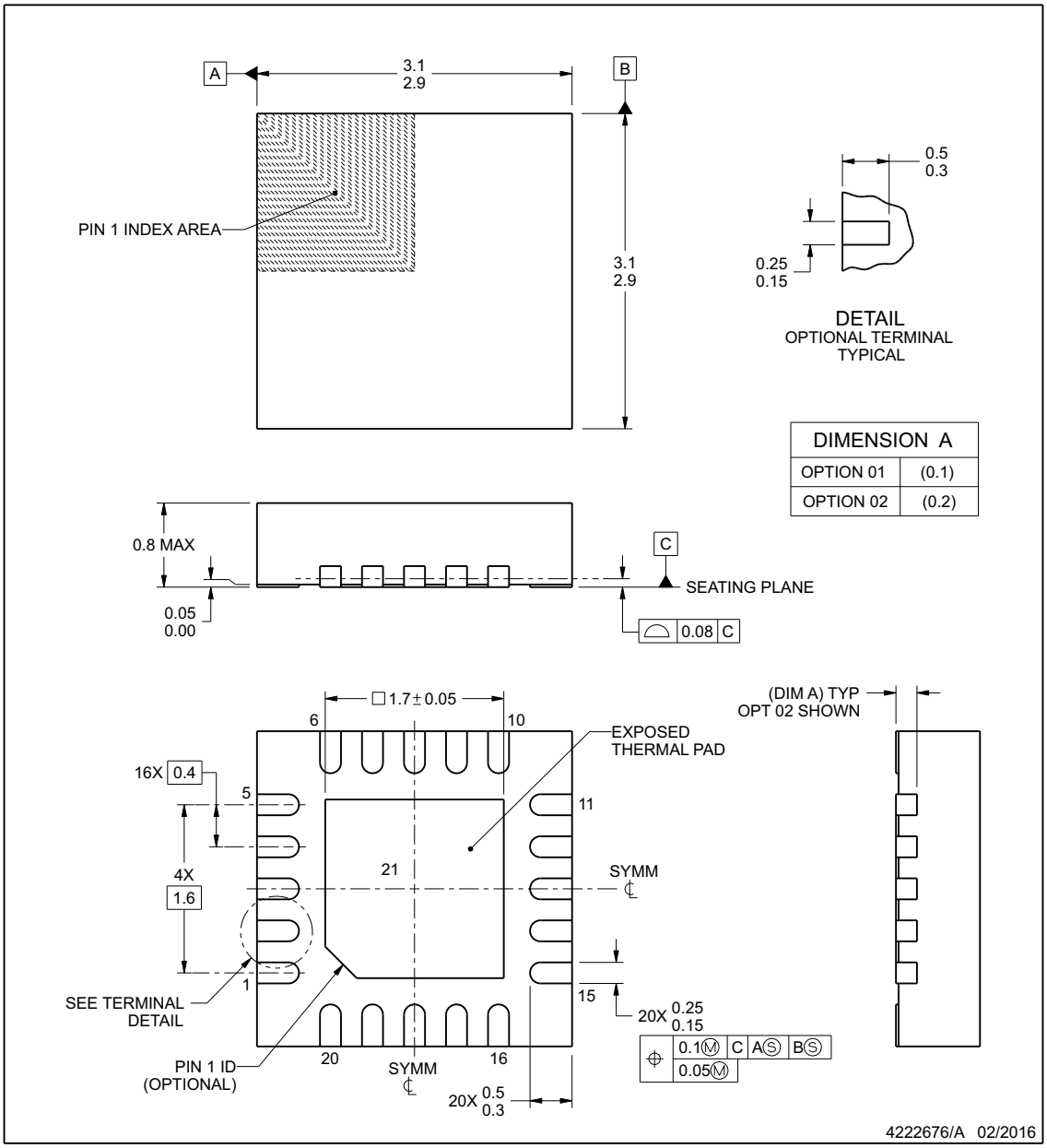
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

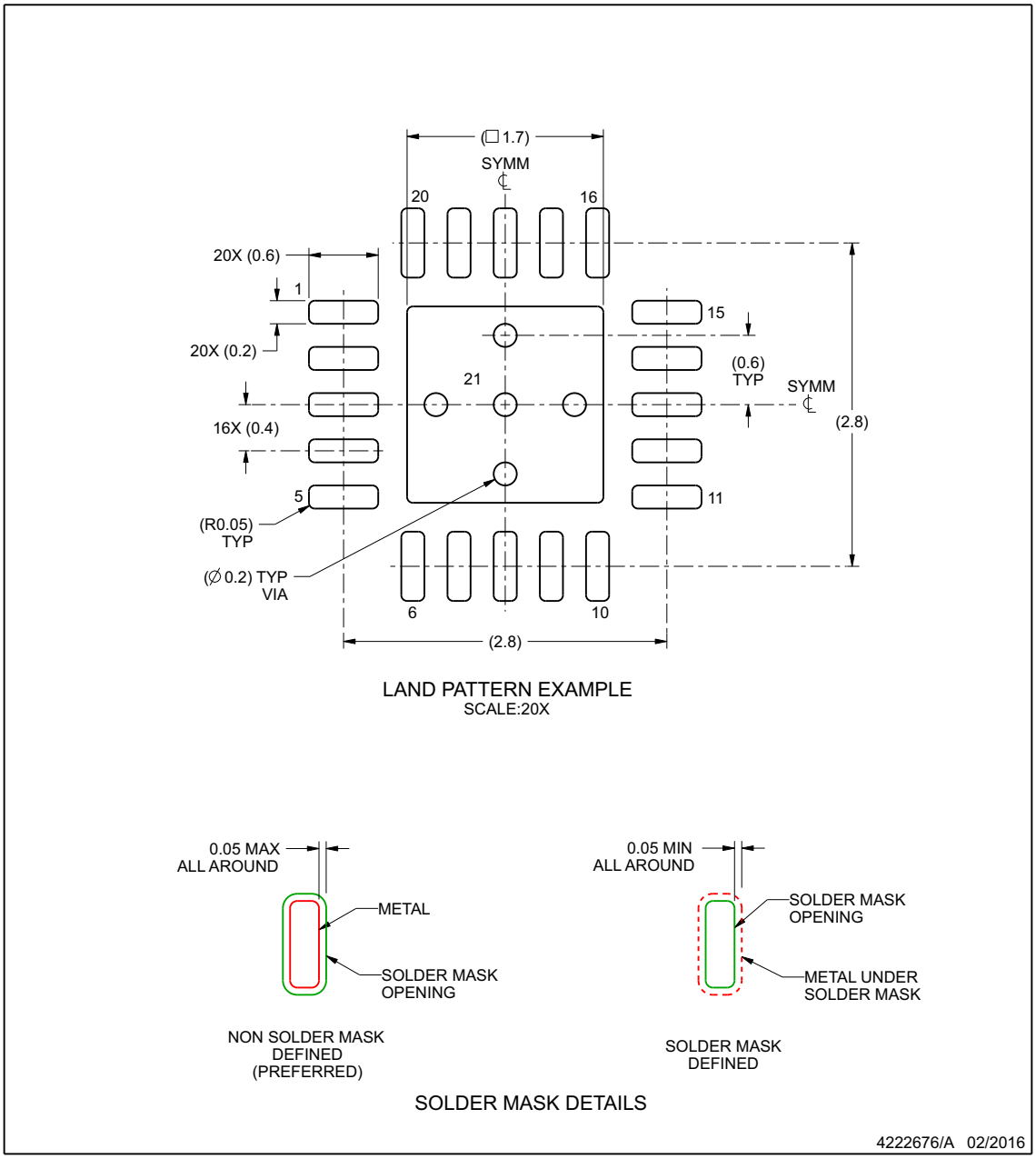
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

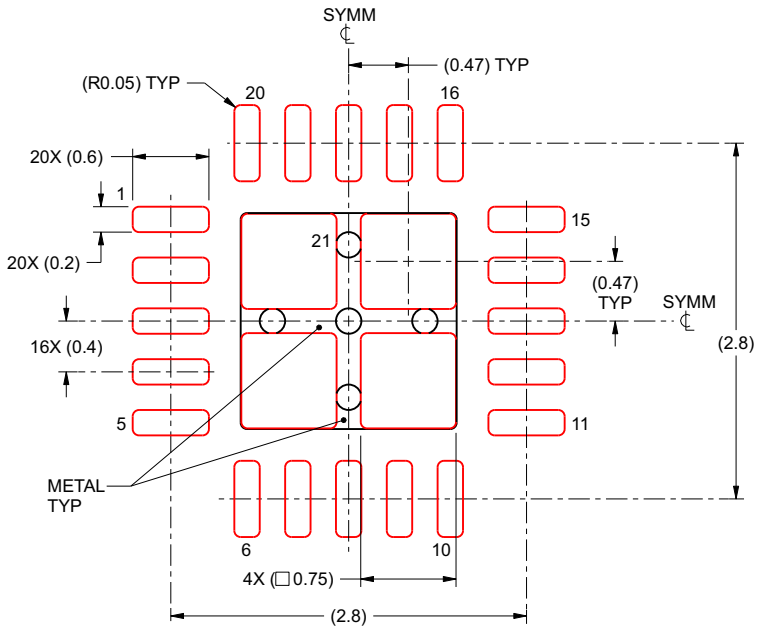
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUK0020B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PADS127L11IPWR	ACTIVE	TSSOP	PW	20	2000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

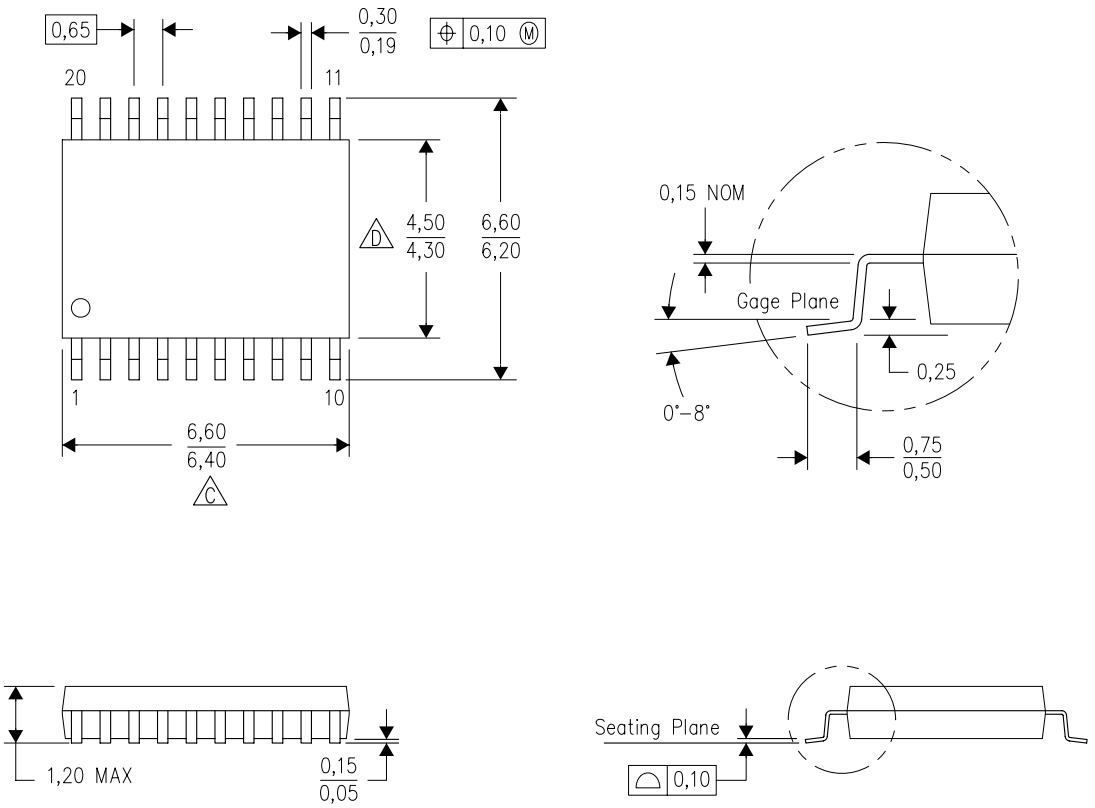
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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