Fig1

Electrical Specifications

Parameter	Conditions	Value
Average current[10]	Update interval 2 s	19 mA
Max. current	During measurement	75 mA
DC supply voltage (V_{ddmin} - V_{ddmax})	Min. and max. criteria to operate SCD30	3.3 V – 5.5 V
Interface	-	UART (Modbus Point to Point) and I²C
Input high level voltage (V_{IH})	Min. and max. criteria to operate SCD30	1.75 V – 5.5 V
Input low level voltage (V_{IL})	Min. and max. criteria to operate SCD30	- 0.3 V – 0.9 V
Output low level voltage (V_{OL})	I_{IO} = +8 mA, Max. criteria	0.4 V
Output high level voltage (V_{OH})	I_{IO} = -6 mA, Min. criteria	2.4 V

Table 4 SCD30 electrical specifications

Fig2

5.3 DC Characteristics (3.3 V, 25 °C)

Table 6: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter		Min	Typ	Max	Unit
C_{IN}	Pin capacitance		-	2	-	pF
V_{IH}	High-level input voltage		0.75×VDD[1]	-	VDD[1]+0.3	V
V_{IL}	Low-level input voltage		–0.3	-	0.25×VDD[1]	V
I_{IH}	High-level input current		-	-	50	nA
I_{IL}	Low-level input current		-	-	50	nA
V_{OH}	High-level output voltage		0.8×VDD[1]	-	-	V
V_{OL}	Low-level output voltage		-	-	0.1×VDD[1]	V
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, output drive strength set to the maximum)	VDD3P3_CPU power domain [1, 2]	-	40	-	mA
		VDD3P3_RTC power domain [1, 2]	-	40	-	mA
		VDD_SDIO power domain [1, 3]	-	20	-	mA

Symbol	Parameter	Min	Typ	Max	Unit
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, output drive strength set to the maximum)	-	28	-	mA
R_{PU}	Resistance of internal pull-up resistor	-	45	-	kΩ
R_{PD}	Resistance of internal pull-down resistor	-	45	-	kΩ
V_{IL_nRST}	Low-level input voltage of CHIP_PU to power off the chip	-	-	0.6	V

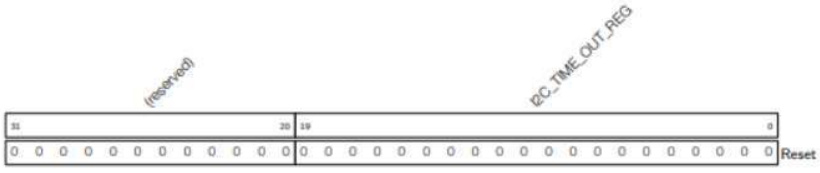
Fig3

1.1 I2C Protocol

Maximal I2C speed is 100 kHz and the **master has to support clock stretching**. Clock stretching period in write- and read-frames is 12 ms, however, due to internal calibration processes a maximal clock stretching of 150 ms may occur once per day. For detailed information to the I2C protocol, refer to NXP I2C-bus specification[1]. SCD30 does not support repeated start condition. Clock stretching is necessary to start the microcontroller and might occur before every ACK. I2C master clock stretching needs to be implemented according to the NXP specification. The boot-up time is < 2 s.

Fig4

Register 11.4: I2C_TO_REG (0x000c)



I2C_TIME_OUT_REG This register is used to configure the timeout for receiving a data bit in APB clock cycles. (R/W)