Camera specification

Osiris M

1 Revision History

Version	Date	Modifications	Author
0.0.1	19/10/2019	Document Creation	A. Gomes
0.0.2	29/01/2021	Updates according to new Spec	C. Claußen
1.0.0	19/03/2021	Updated electrical and optical spec tables; added defect pixel definition and optical QE graphs,	F.Gaspar
1.0.1	18/10/2021	p. 39 “Rows in Delay Calculation *16 instead of *8”	C. Claußen
1.1.0	17/05/2022	Updated several parameters in “Operating conditions” and “electrical characteristics”. Revised calculations in timings (exposure and integration and others)	F.Gaspar

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3 Introduction

Osiris M is a small form factor image sensor for space restricted applications. It has a high sensitivity rolling shutter pixel with large full well capacitance, specially designed for medical endoscopic applications where high SNR is mandatory. The sensor has a high frame rate to permit SNR enhancement and smooth, low delay display on a wide range of display interface standards.

The sensor features on chip 10bits ADC and a bit serial data interface over LVDS data line. The data line is semi duplex such that configuration can be communicated to the sensor in the frame brake. Optionally the interface can be switched to single ended LVTTL interface, with data clock and serial data on the two LVDS data lines. In the single ended interface mode (SEIM), the device will be in Slave configuration.

The exposure time and analogue gain can be programmed over the serial configuration interface.

4 Disclaimer

The Integrated Circuit (IC) and its parts have been or will be designed and developed so as to conform in all material respects to the preceding introduced specification based on the performance indication and guideline from the silicon manufacturer regarding the target CMOS technology.

Optasensor GmbH reserves the right of changing or update the specification at any time. When designing this product into a system, it is necessary to check for updated information and availability.

This product is intended for use in commercial range applications, excluding extended temperature range, reliability applications or harsh environments, such as military, medical life-support or life-sustaining equipment. Any of such applications is not recommended without additional processing and written agreement from Optasensor GmbH.

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Any change to the specification shall be mutually consulted and determined with the prior written consent of the parties. Any changes to the specifications required by the Customer shall be mutually agreed upon and laid down in writing as a supplement to or correction of the specifications.

5 General Statements and Conventions

Text in this document between "{info only:" and "end info}" or "{" and "}" is for information only. Parameters and information given in this section contain background information. Performance and parameters given in these sections cannot be guaranteed. No implicit nor explicit specification can be derived from these sections.

5.1 Tolerances

For all parameters, nominal value, upper, and lower bound of guaranteed specification are indicated. Parameters indicated without tolerances are for info only and cannot be guaranteed.

5.2 Power supply

The lowest supply voltage in the chip is referred to as VSS. VSSxx indicates the lowest power supply voltage of a sub block xx of the circuit. All VSS power supply has the same potential at all pins at any time.

The highest supply voltage of a sub block xx of the circuit is referred to as VDDxx. All pins carrying identical VDDxx power supply net labels have the same potential at any time, neglecting parasitic effects.

All voltage specifications are referred to VSS unless otherwise specified. All positive currents flow into a pin. The sinking of current means that current is flowing into a pin. The sourcing of current means that current is flowing out of a pin.

5.3 Clock specification

All timing information treated by a digital control part refers to the master clock frequency unless otherwise specified. Depending on the interface mode, the master clock frequency is generated by the on-chip oscillator or provided over the clock line in the single ended interface mode, on the CLK pin.

5.4 Digital Numbers

Whenever referred to the output signal this is indicated in DN (Digital Numbers) equalling 1 unit (1LSB) of the on-chip ADC. This quantity is sometimes also referred to as "grey levels".

6 Block Diagram

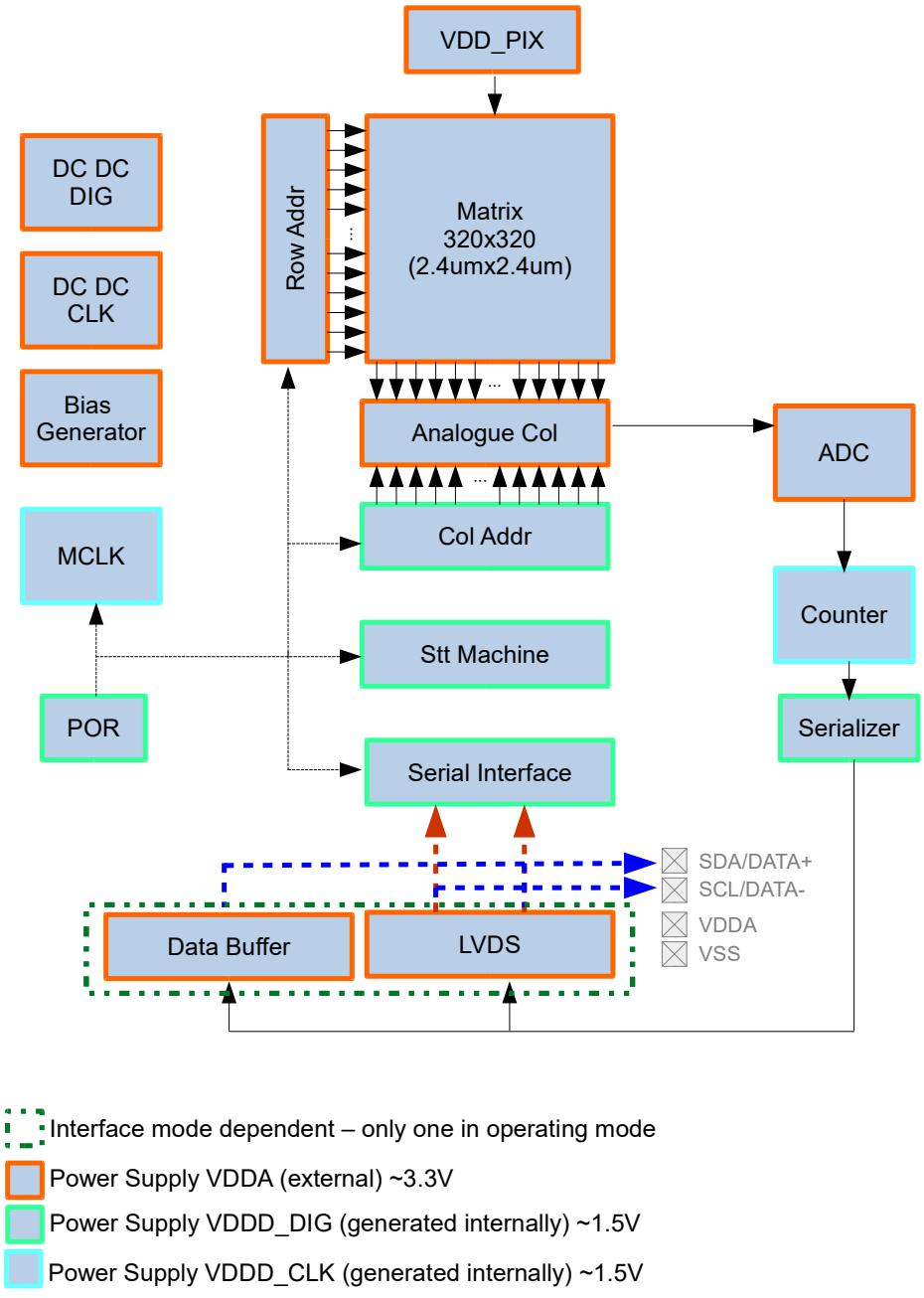


Figure 1: Block Diagram.

7 External Components

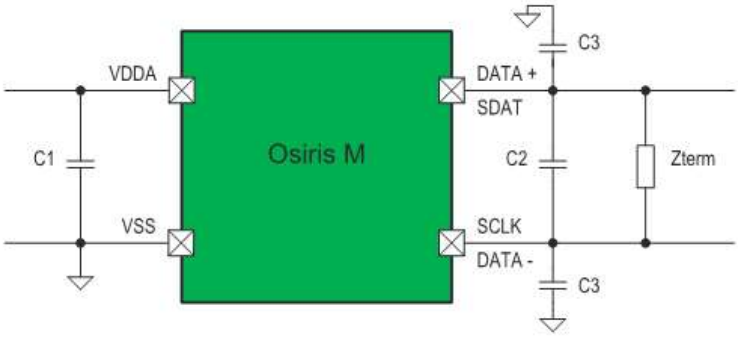


Figure 2: External Components – LVDS mode.

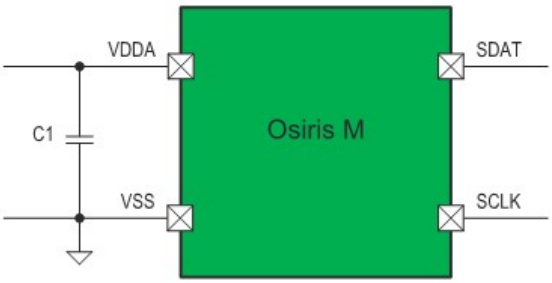


Figure 3: External Components – SEIM.

Legend External components:

Component	Description	Nominal Value
C1	Power supply decoupling	>100nF
C2	Differential load on LVDS lines (parasitics)	< 3pF
C3	Single ended load on LVDS lines (parasitics)	< 5pF
zRterm	Impedance of LVDS termination (only in case of LVDS interface mode, leave open otherwise)	120 Ohm

Table 1: External components

8 Electrical Description

The sensor will comply with the specifications listed in this section within the operating ranges listed in the respective section.

An applied signal must not have a deviation from the ideal signal, at the pin of the circuit, such that the circuit or the parameter under test are affected significantly.

Proper decoupling of the circuit according to section 7 is required. The following section defines the limits of functional operation and parametric characteristics of the circuit, and reliability. Note that functionality of the circuit outside the operating range as specified in this section is not guaranteed.

8.1 Absolute Maximum Ratings

Stresses above those listed in this clause may cause immediate and permanent device failure. Operation outside the operating conditions for extended periods may affect device reliability. It is not implied that more than one of these conditions can be violated simultaneously.

Symbol	Description	Min	Max	Unit
VDD	Power supply voltage	-0.5	3.6	V
VIO	Voltage on any IO	-0.5	3.6	V
IIO	DC forward BIAS current, input or output		1	mA
RH_{NC_STRG}	Long term storage humidity	0	60%	
t_{STRG}	Maximum storage time		3	years

Table 2: Absolute Maximum Ratings

8.2 Electrical overstress immunity

The device withstands 2KVolts ESD pulses when tested according to JEDEC JS-001-2017.

8.3 Operation conditions

Functional operation is guaranteed under these conditions.

Symbol	Description	min	typical	max	unit
V_{DDA}	Power supply voltage (analogue)	3.2	3.3	3.4	V
$VN_{rms}V_{DDA}$	RMS Noise on VDDA			5	mV
$VN_{pp}V_{DDA}$	Peak to Peak Noise on VDDA			20	mV
T_A	Ambient Temperature for operation	15	38	55	°C
RH_{NC}	Relative humidity (non-condensing)	5%		85%	
T_{strg}	Storage temperature range	-40		30	°C
MSL_{Module}			N.A.		

Table 3: Operation Conditions

8.4 Electrical characteristics

Symbol	Description	min	typ	max	unit

Int_Time	Programmable integration time (main clock default)	0.13	-	261	ms
P_{clk_std}	Internal pixel clock (by programming register, MCLK_MODE_REG[1:0] and HIGH_SPEED_REG[0], see section 11.2)		1.03 2.05 4.09		MHz
P_{clk_HS}	Internal pixel clock (by programming register, MCLK_MODE_REG[1:0] and HIGH_SPEED_REG[0], see section 11.2)		1.31 2.59 5.22		MHz
$P_{LVDSmode}$	Total of power consumption (Idle mode Off, MCLK = 31MHz; see section 11)		12		mW
$P_{LVDSmode}$	Idle mode = ON		3.2		mW
Single Ended Mode Interface					
$t_{slew,\ rising}$	Input slew rate of rising edge		3		ns
$t_{slew,\ falling}$	Input slew rate of falling edge		3		ns
MCLK	Input clock for SEIM		60	75	MHz
$I_{sdat,\ sclk}$	SEIM output signal current (set by register bits output_curr[1:0])		3.9 … 9.6		mA
LVDS downstream interface					
V_{CM}	Data common mode output voltage	1	1.4	1.8	V
$I_{DATA+,DATA-}$	LVDS signal current (set by register bits output_curr[1:0])	600	600 1200 2000	2000	uA
B_{CLK_STD}	Bit clock for serial data transmission (12PCLK, set by register bits mclk_mode[1:0] and high_speed[0])	12	12 25 49	49	MHz
B_{CLK_HS}	Bit clock for serial data transmission high speed (12PCLK, set by register bits mclk_mode[1:0] and high_speed[0])	16	16 31 63	63	MHz
J_{DATA}	Jitter data clock	-20%		20%	
LVDS $_{swing}$	Differential signal swing peak to peak with $Z_{diff} = 120\Omega$	72		240	mV
$t_{slew,\ rising}$	Output slew rate of rising edge		3		ns
$t_{slew,\ falling}$	Output slew rate of falling edge		3		ns
Digital Upstream Interface					
V_{IL}	SCLK, SDAT low level input voltage	- 0.3		0.4	V

V_{IH}	SCLK, SDAT High level input voltage	VDDA - 0.3		VDDA + 0.3	V
t_S	Setup time for upstream configuration relative to SLCK	3			ns
t_H	Hold time for upstream configuration relative to SLCK	3			ns
f_{SCL_LVDS}	SCLK frequency in LVDS			2.5	MHz

_std → assuming High Speed bit Off
_hs → assuming High Speed bit ON

Table 4: Electric Characteristics

8.5 Electro Optical characteristics

These parameters were measured at 530nm and MCLK 25MHz and calculations are according to EMVA 1288 release 3.1

Parameter	**RGB**	**Mono**	**Unit**
Pixel Size/Pitch x/y	2.4	2.4	um
Pixel Size/Pitch y	2.4	3.4	um
Number of pixels in x direction	320	320	pixels
Number of pixels in y direction	320	320	pixels
Total number of pixels	102400	102400	pixels
DSNU	0.84	0.84	DN
PRNU	1.3	1.7	%
Responsivity	8.9	6.61	DN/nJ/cm^2
Dynamic Range	61.3	60	dB
SNR max	38.4	38.4	dB
Conversion Gain	0.136	0.137	DN/e-
Temporal read noise in dark	0.73	0.84	DN
Dark noise	5.3	6.1	e-
Full Well capacity	6.2	6.2	ke-
Total QE @ 530nm	42.5	31.4	%

Table 5: Optical Characteristics

These parameters were measured at 530nm and MCLK 25MHz and calculations are according to EMVA 1288 release 3.1.

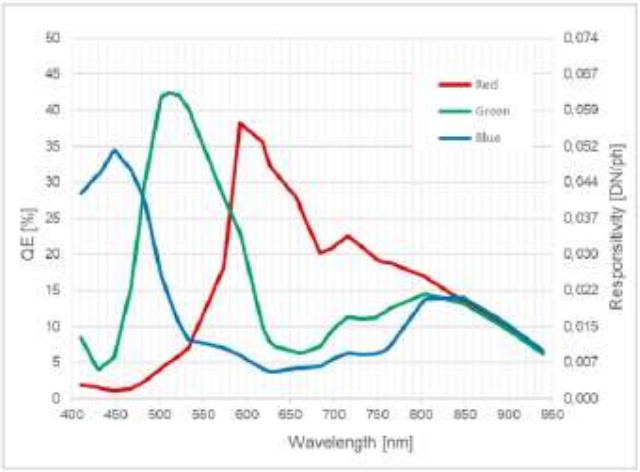


Figure 4: QE and responsivity for RGB sensors

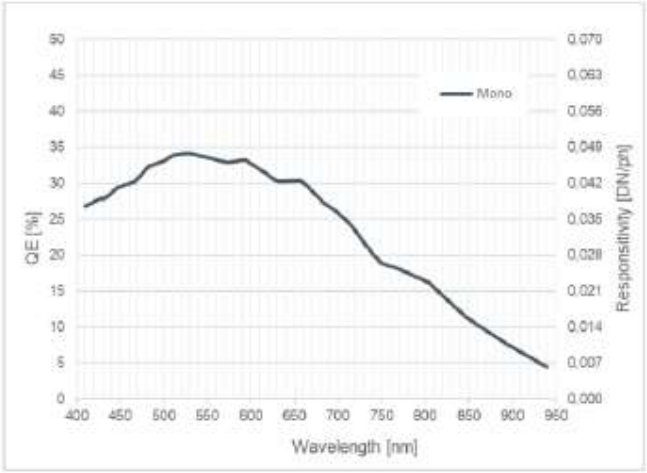


Figure 5: QE and responsivity for B&W sensors

Defect designation	Definition
Defect pixel in dark images	Pixel values differ more than 50DN to the median of full image, excluding the first and last 2 rows and columns
Defect pixel in gray images	Pixel values differ more than 4 sigma from mean of 7x7 neighbors, calculated in the image center, for an image mean between 300 to 700DN in that region

Defect pixel in saturation images	Pixel values differ more than 50DN from the median of the full image, excluding the first and last 2 rows and columns, with a mean image above 1000DN
Defect pixel cluster	Any region of 5x5 pixels that includes more than 1 defect pixel according to defect pixel definitions

Table 6: defect pixel definition

9 Summary of sensor specification parameters

Parameter	Osiris M Sensor	Comments
Active Pixel matrix	320 x 320	FSI, 4T, 2pixel vertically shared
Pixel size	2.4um x 2.4um	
Optical format	1/15”	
Chip Size	1.05mm x 1.05mm	±0.06mm
Fill factor	45 %	
Shutter mode	Rolling shutter	Adjustable Integration time
ADC Resolution	10bits	
Gain	0.8x / 1x/ 1.3x / 2x	Analog
Exposure time	0.13 to 261ms	
Number of defect pixels	<10	According to Table 6: defect pixel definition, with 3.3V supply and register 0 = 0x009D and register 1 = 0x0164
Defect pixel cluster	0	
Response curve	Linear	
Frame Rate	4 – 38fps (or 5 to 49fps in HS mode)	Programmable changing the main clock configuration
Number of pads	4	VDDA, VSS, DATA+/SDA and DATA-/SCL
Data interface	Single Ended with 12bits	Slave mode, with clock provided externally
	LVDS signal with 12bits	
Operation Mode	Free running	
Power consumption	12mW (LVDS mode) 9.7mW 25MHz (SEIM) 3.2mW Idle mode	It is possible to set an Idle Mode to reduce the power consumption

Table 7: Summary of specification parameters

10 Functional Description

10.1 General sensor description

The outlined sensor is used for area scan applications with rolling shutter, and the pixel architecture used in this sensor is a 4T photo diode, with two pixels vertically shared. It has 320 pixels x 320 pixels.

The sensor provides two different operation modes, selectable over the serial interface:

1) **LVDS** – Fully self-timed operation in a free running master mode with LVDS downstream data transmission and Single Ended Interface upstream communication, time multiplexed. During transfer of the image data, the pixel values are transmitted in bit serial manner with 12 bits and embedded clock using Manchester coding [start bit (1-bit) + data (10bits) + stop bit (1-bit)].
2) **SEIM** – **Single Ended Interface Mode**, fully self-timed operation in free running slave mode with Single Ended Interface downstream data transmission and Single Ended Interface upstream communication, time multiplexed. The DATA+ line carries the data while DATA- line transmits the clock. The data word coding with start bit (1-bit) + data (10-bit) + stop bit (1- bit) is the same as in the LVDS mode.

After power up, the sensor performs an internal power on reset, and then remains in idle mode with active upstream Serial Interface Mode, until the operation mode is selected and request to leave idle mode.

The integration time can be programmed by defining the number of rows in reset and/or programming the delay mode time. Since default frame rate is 23 full frames per second (FPS) the maximum integration time is 1/FPS[s] (~53ms, considering minimum time for delay mode and minimum number of rows in reset, ROWS_DELAY_REG[4:0] and ROWS_IN_RESET_REG[6:0] register setting).

Due to the small chip size only four pads are available, two for power and two for a bi-directional data interface. Sensor configurations are performed over a Differential Serial Interface available on the same 2 pins used for data communication (LVDS or Single Ended CMOSLVTTL depending on operation mode and/or communication direction).

During transfer of the image data, the pixel values are transmitted in bit serial manner over an LVDS or single ended channel. In LVDS mode the clock is embedded in the data by using Manchester coding. The data is completed by a start bit and a stop bit for easier de-serialization, (*start bit (1bit) + data (10bits) + stop bit (1bit)*). The architecture allows a full linear AD conversion of 10 bits, with a programmable conversion gain.

After each frame, the data interface is switched for a defined time to upstream configuration interface, where the positive LVDS channel holds the serial configuration data and the negative

channel holds the serial interface clock, on LVDS mode. On Single Ended Mode, the clock transmitted over negative channel should be maintained, and the positive channel will be used to change configuration and data transmission.

The sensor switches fully self-timed between the downstream and the upstream mode. Therefore it is the user responsibility to tristate the drivers for upstream serial configuration link prior to start of data transmission from the sensor. Due to the limited current output from the sensor, it is not expected that conflicting drive of the data lines will permanently destroy the device, however this condition would seriously degrade the data integrity and is not qualified in terms of device reliability and lifetime.

If required, the sensor data rate can be modulated slightly by adjusting the sensor supply voltage, because the frame rate is linear dependent of the main clock. If multiple sensors are to be synchronized, this is possible by individually modulating the sensor power supply to match each sensors operation frequency.

In SEIM, the sensor operates synchronous to the provided clock on the SCL line (negative data line). It is the user responsibility to assure in this operation mode that the provided external clock frequency does not exceed the maximum allowed clock frequency. Lower clock frequencies are possible. While functionally it may be possible to hold the provided clock, artefacts may occur if the clock frequency is not fixed during operation.

10.2 Sequence of operation

Osiris M sensor will start in INTERFACE MODE waiting for configuration and request to leave idle mode. After the request the sensor will go to a loop of 4 modes, which are described below:

- INTERFACE MODE: during this mode, which is active during 648 PP it is possible to write and update the register configuration. In this mode DATA pins are used as SDA and SCL.
- SYNC MODE: during this mode the sensor is transmitting training pattern to allow the sensor synchronization (duration of 657 PP).
- DELAY MODE during this mode the sensor will keep the state before during the programmed time, sync pattern is also sent during this mode. It can be programmed between 2 to 498 row periods.
- READOUT MODE: during this mode the sensor assumes that the synchronization is done and starts to send image data, the pixel values are transmitted in bit serial manner over an LVDS channel with embedded clock, or single ended depending on the selected transmission mode. Note that before each row a Start Line identification is sent with the duration of 8 PP and that after the last row an *End Of Frame* is sent with the duration of 7 PP.
    - Each row data has:
        - 8 PP – start line identification
        - 320 PP – image data

- At the end of the last row data (End Of Frame)
  - 7 PP – end frame identification

The sensor transmits the synchronization pattern during at least four row clock periods correspondent to the *sync_mode* and to the *delay_mode* (if is set the minimum programmable value) but it can transmit the pattern continuously during more time according to the *delay_mode* value programmed, which can go from 2 to 498 row clock period (2*328 to 498*328).
Note: PP refer to Pixel Period

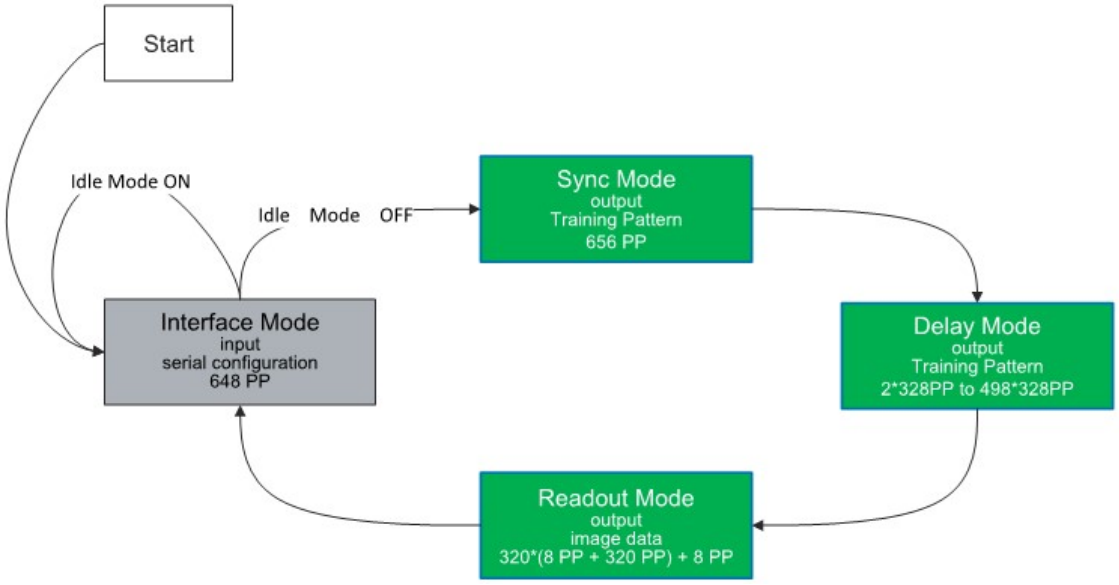


Figure 6: Sequence of operations.

Phase Nbr	***Status***	***Start bit***	***Data EXOR with clock***	***Interface Status***	***Duration in Pixel Period***	***Comment***
Interface Mode						
SERIAL	Time for Serial configuration	N/A	N/A	S_INT IN	648 PP (*)	Serial Interface
Sync Mode						
SYNC	Transmission of continuous 0	no	yes	LVDS OUT	328*2 PP	re-synchronism
Delay Mode (programmable)						

DELAY	Transmission of continuous 0	no	yes	LVDS OUT	328*2 PP to 328*498 PP	Programmed delay
Readout Mode						
RD R1.1	Transmission of continuous 0	no	yes	LVDS OUT	8 PP	Image data start line
	Transmission of 320 pixel values	yes	yes	LVDS OUT	320 PP	Image data (Row 1)
RD R1.2	Transmission of continuous 0	no	yes	LVDS OUT	8 PP	Image data start line
	Transmission of 320 pixel values	yes	yes	LVDS OUT	320 PP	Image data (Row 2)
RD R2.1	Transmission of continuous 0	no	yes	LVDS OUT	8 PP	Image data start line
	Transmission of 320 pixel values	yes	yes	LVDS OUT	320 PP	Image data (Row 3)
RD R2.2	Transmission of continuous 0	no	yes	LVDS OUT	8 PP	Image data start line
	Transmission of 320 pixel values	yes	yes	LVDS OUT	320 PP	Image data (Row 4)
Readout of all rows						
RD R160.1	Transmission of continuous 0	no	yes	LVDS OUT	8 PP	Image data start line
	Transmission of 320 pixel values	yes	yes	LVDS OUT	320 PP	Image data (Row 319)
RD R160.2	Transmission of continuous 0	no	yes	LVDS OUT	8 PP	Image data start line
	Transmission of 320 pixel values	yes	yes	LVDS OUT	320 PP	Image data (Row 320)
RD EOF	Transmission of continuous 0	no	no	LVDS OUT	8 PP	End of frame

(*)When Idle Mode is Off. If Idle Mode is enabled the sensor remains on this working mode until disable the Idle Mode

Table 8: Sequence of operation

10.3 Matrix Readout

To guarantee a high fill factor a pixel layout was developed with the two vertical pixels electronics shared.

The Matrix readout is according to the following sequence:

- Read first row (R1.1), starting in the position (1;1) and finishing in the position (1;320)

- Read second row (R1.2), starting in the position (2;1) and finishing in the position (2;320)
- Read last row (R160.2), starting in the position (320;1) and finishing in the position (320;320)

Note: (row, column), i.e., (2;1) represents row 2 column 1.

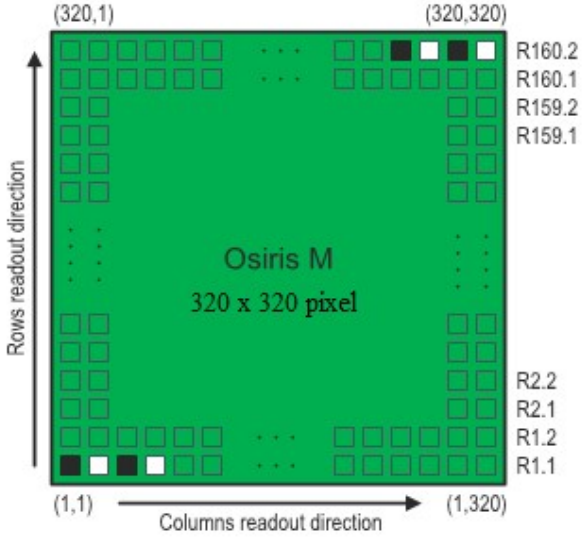


Figure 7: Matrix readout sequence.

Note that, first four and last four pixels have a specific pattern, they are black and white pixels, to allow corrupt frames detection.

10.4 Integration and rolling shutter

Integration is defined based on the number of rows in reset, defined by user. Matrix is processed with rolling shutter, which means one row is selected for readout while a defined number of previous rows are in reset, and all the other rows are in integration.

Note that a delay mode in the beginning of each frame can be added to increase the integration time.

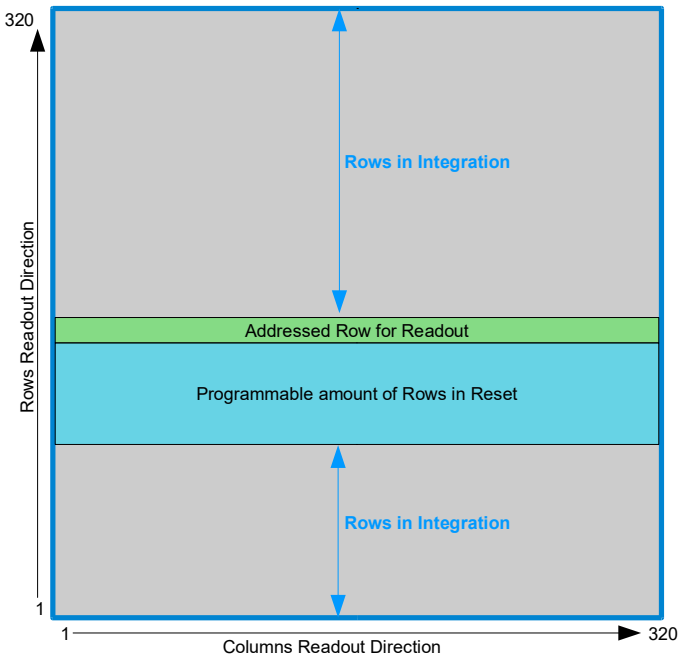


Figure 8: Matrix readout sequence.

According to this, it is now possible to define the maximum and the minimum total integration time:

$$IntegrationTime = row_{\text{btw\_frame}} + rows_{nbr} - rows_{\text{in\_rst}} - row_{\text{in\_readout}}$$

The variables below are defined in number of Pixel Periods (PP) per phase, according to table 6:

→ $\boldsymbol{row_{btw\_frame}}$: number of rows between frame is	
$row_{\text{btw\_frame}} = rows_{spi} + rows_{sync} + rows_{delay}$	
$rows_{spi}$	$rows_{spi} = 648PP$
$rows_{sync}$	$rows_{sync} = 2 * 328PP = 656PP$
$rows_{delay}$	$rows_{delay} = (16 * \text{ROWS\_DELAY\_REG}[4:0] + 2) * 328PP$ ROWS_DELAY[4:0] is the value programmed for delay mode (see section 11.2)
→ $\boldsymbol{rows_{nbr}}$: it is always 320, each row has 328PP (Pixel Period)	
$rows_{nbr} = 320 * 328PP = 104960PP$	
→ $\boldsymbol{rows_{in\_rst}}$: number the rows in reset	

$rows_{\text{in\_rst}} = (2 * \text{ROWS\_IN\_RST\_REG}[7:0] + 2) * 328PP$ ROWS_IN_RST[7:0] it is a programmable value (see section 11.1). Maximum value is equal to the total of number of sensor rows.
→ ***row*$_{in\_readout}$**: time to access a specific row for readout
$row_{\text{in\_readout}} = 2 * 328PP = 656PP$

Table 9: Integration time- variables definition

The maximum and minimum integration time is defined by:

Assuming ROWS_DELAY_REG[4:0]= '00000' $rows_{delay} = (16 * 0 + 2) * 328PP = 656PP$ $row_{\text{btw\_frame}} = 648PP + 657PP + 656PP = 1961PP$	
ROWS_IN_RST_REG[7:0] = '00000000' (0) $rows_{\text{in\_rst}} = 2 * 328PP = 656PP$	$IntegrationTime_{maximum} = 1961PP + 104960PP - 656PP - 656PP$ $IntegrationTime_{maximum} = 105609PP$
ROWS_IN_RST_REG[7:0]= '101000000' (160) $rows_{\text{in\_rst}} = 322 * 328PP = 105616PP$	$IntegrationTime_{minimum} = 1961PP + 104960PP - 105616PP - 656PP$ $IntegrationTime_{minimum} = 649PP$
Assuming ROWS_DELAY_REG[4:0] = '11111' $rows_{delay} = (16 * 31 + 2) * 328PP = 163344PP$ $row_{\text{btw\_frame}} = 648PP + 657PP + 163344PP = 164649PP$	
ROWS_IN_RST_REG[7:0] = '00000000' (0) $rows_{\text{in\_rst}} = 2 * 328PP = 656PP$	$IntegrationTime_{maximum} = 164649PP + 104960PP - 656PP - 656PP$ $IntegrationTime_{maximum} = 268297PP$
ROWS_IN_RST_REG[7:0] = '101000000' (160) $rows_{\text{in\_rst}} = 322 * 328PP = 105616PP$	$IntegrationTime_{minimum} = 164649PP + 104960PP - 105616PP - 656PP$ $IntegrationTime_{minimum} = 163337PP$

Table 10: Integration time – maximum and minimum

{info only:
An example to illustrate the use of the above formulas, the maximum and minimum integration time is calculated in the table below:

ROWS_DELAY _REG[4:0]	ROWS_IN_RST _REG[7:0]	Integration Time maximum and minimum
00000'b	00000000'b	$IntegrationTime_{maximum} = 105609PP$
	10100000'b	$IntegrationTime_{minimum} = 649PP$
11111'b	00000000'b	$IntegrationTime_{maximum} = 268297PP$
	10100000'b	$IntegrationTime_{minimum} = 163337PP$

Table 11: Integration time – maximum and minimum assuming main clock configuration modes (High Speed Off)

ROWS_DELAY _REG[4:0]	ROWS_IN_RST _REG[7:0]	Integration Time maximum and minimum
00000'b	00000000'b	$IntegrationTime_{maximum} = 105609PP$
	10100000'b	$IntegrationTime_{minimum} = 649PP$
11111'b	00000000'b	$IntegrationTime_{maximum} = 268297PP$
	10100000'b	$IntegrationTime_{minimum} = 163337PP$

Table 12: Integration time – maximum and minimum assuming main clock configuration modes (High Speed On)

:end info}

Note that each pixel from a row is processed according to the following steps:

→ Integration

→ Readout (RD)

→ Reset

Bellow an example of sensor functionality assuming:

Minimum Delay mode:

ROWS_DELAY_REG[4:0]= '00000', It is 2 rows in delay

Rows in Reset:

ROWS_IN_RST_REG[7:0]= '00000010', It is 6rows in reset

On Figure 9, it is possible to see:

- The operation mode of the sensor in each state

- The status of the rows (Row 1.1 and Row 1.2)

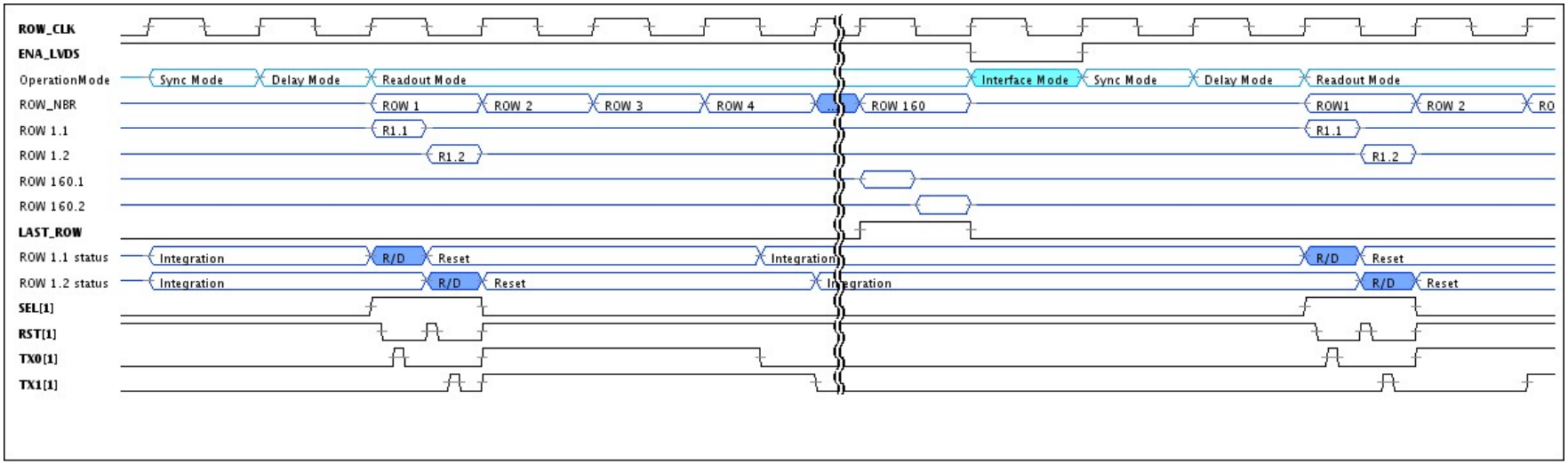


Figure 9: Integration time, assuming 2 rows in delay mode and 6 rows in reset.

Note: Update this figure to include the new starting phase (Interface mode)

10.5 ADC

It is a 10bits full linear ADC. The architecture of the ADC allows programming several items:
→ Voltage Reference for signal (VREF_REG[1:0] , Register 1)
→ Ramp Gain (RAMP_GAIN_REG[1:0] , Register 0)
→ Ramp Offset Voltage (OFFSET_RAMP_REG[1:0] , Register 0)
→ CDS gain (CDS_GAIN_REG[0] , Register 1)
→ CDS current (bias_curr_increase[0], Register 1)

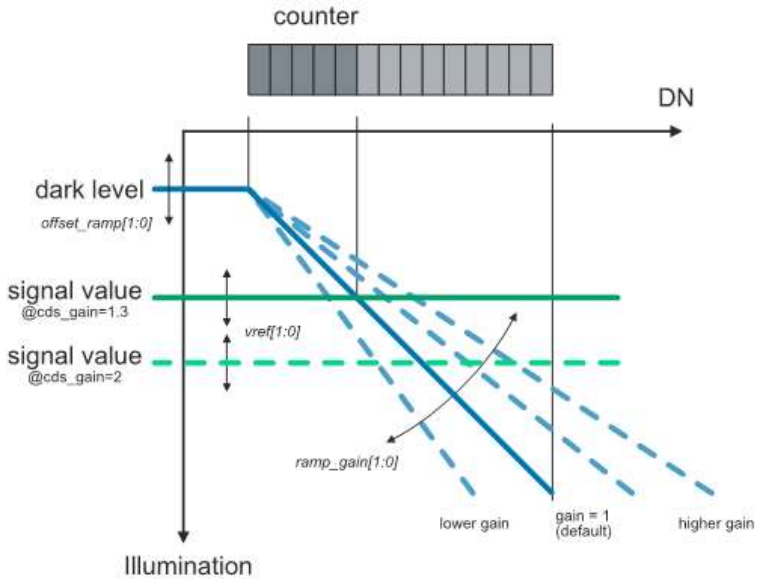


Figure 10: ADC configurable values.

See detailed information about the configurable values in section 11 .

10.6 Interfaces

This sensor features a semi duplex data interface which shares the LVDS bit serial downstream channel with the SPI register configuration channel used for upstream of configuration data to the sensor. This needs a synchronization every time it passes from the upstream to a new downstream mode at the image receiver side.

By register configuration the downstream interface can be chosen to be LVDS type with the serial data EXOR combined with the Bit Clock (Manchester code) or to be single ended.

In SEIM the negative data line is always configured as a LCCMOSTTL input and receives the bit clock. The pixel clock is internally generated by means of diving this clock by12. The serial transmission is directly clocked by the provided clock signal, and a new bit is transmitted on each rising edge of the received clock. As the on-chip ADC will still run on the on-chip oscillator, it is the user responsibility to assure the provided clock does not exceed 90% of the nominal clock frequency as a function of the clock division bits given by the table on section 11.2 .

During the communication break, the clock must be continuously provided. Outside the upstream data communication, the data line must be driven in tristate mode.

The SEIM is only suitable for applications where the data receiver is placed very close to the sensor chip. For any application where the sensor is used with connection cable between the sensor and the receiver, the use of the LVDS mode is recommended. In SEIM the bit serial data stream is not EXOR combined with the bit clock.

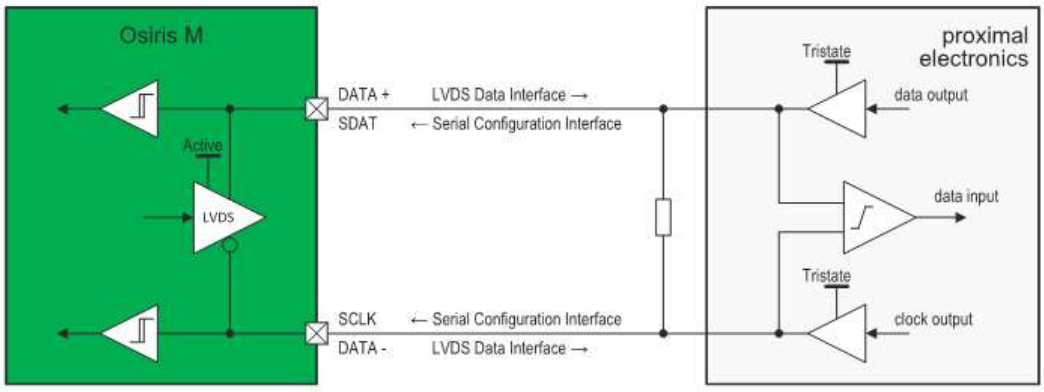


Figure 11: LVDS mode communication interface.

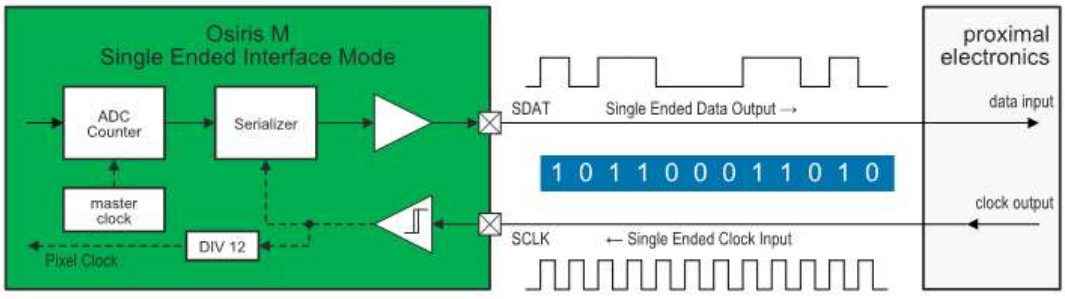


Figure 12: SEIM communication interface.

10.6.1 Serial Configuration

The serial configuration is implemented based on a Differential Serial Interface which shares the Data Interface pins, to keep a lower number of pins in the sensor, when in LVDS Mode, or sharing only the data line when in SEIM.

The serial interface consists in upstream data interface of a two 16 bit write only register. The register can be updated between frames, by the *serial data line* – SDA and by the *serial clock line* – SCL external controlled signals. The registers are written by sending a 4-bit update code, followed by a 3 bit register address (only register 000 and 001 are implemented), 16bit register data and a bit fixed to "0".

All data is written MSB to LSB. Data is captured on the rising edge of SCLK. The minimum set-up and hold times for SDA respectively to the rising edge of SCLK are 4ns and 1ns, respectively. However, it is recommended to change SDA on the falling edge of SCLK to guarantee maximum set-up and hold times.

The content of the input shift register is updated to the effective register once a correct update code (1001) has been received and shifted by 24 serial clocks. The input shift register is reset to all 0's, 1 SCLK after the code detection.

The below table indicates the sequence of writing update code, register address and register data.

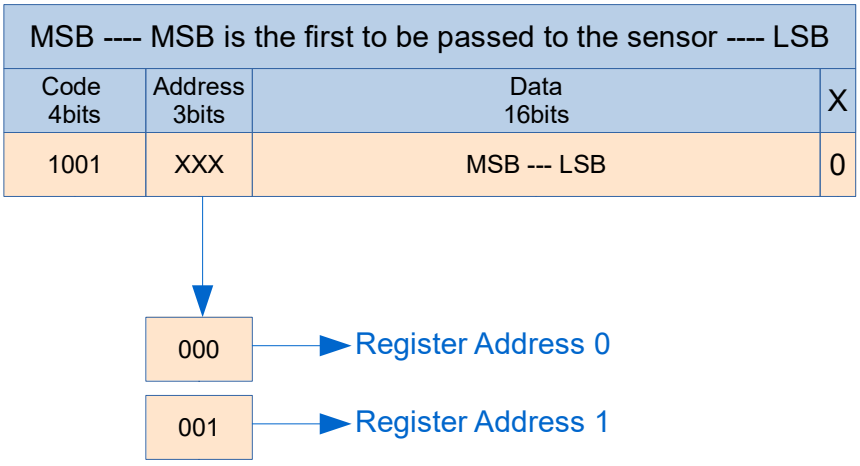


Figure 13: Serial Interface Word.

A correct sequence must have 24 SCLK, where:

- The first 4 SCLK are for detection of a correct code (must be 1001).
- The next 3 SCLK will indicate the register to be written (000 or 001).
- The next 16 SCLK will pass the data information (from MSB to LSB).

- Finally, the last SCLK will pass the bit “0” that is used to separate words.

Note that the maximum frequency of SCLK can go up to 75MHz.

- ***Logic transition levels upstream interface***

When in serial configuration mode, the inputs of the data interface are de-glitched by means of a hysteresis between 1.4V for the high low transition and 1.6V for the low high transition. Thus, for proper logic values the voltage levels of the below table should be respected.

Input voltage range	*Received logic*
0V - 0.4V	0
0.4V – 2.9V	X
2.9V - 3.3V	1

Table 13: Serial interface – Logic levels

In the case of LVDS data transmission, the above decision thresholds have to be considered for the dimensioning of the upstream drivers in the proximal circuitry, since the serial clock and the serial data couple to each other over the LVDS line termination register.

Driving the serial configuration data should be carefully designed along with the cables inductance to avoid signal overshoot at the chip side. It is recommended to use slew rate-controlled drivers with a low slew rate. No distal termination of the data lines is implemented on chip.

10.6.2 Data Interface LVDS transmission mode

The Osiris M image data is generated as 10bit representation. Each pixel data is transmitted in a pixel clock, what means a data bit rate at 12 times the pixel frequency. Then the 12bits pixel data word is done adding a start and stop bit to the 10bits.

Main Clock Configuration (MCLK_MODE_REG[1:0] // HIGH_SPEED_REG[0])	*Description*	*Interface Speed MCLK [MHz]*	*Frame Rate [fps]*
'00' // '0'	Main clock 2x	49.1	38
'01' // '0'	default	24.7	19
'1x' // '0'	Main clock /2	12.3	9

'00' // '1'	Main clock 2x	62.6	49
'01' // '1'	Default high speed	31.1	24
'1x' // '1'	Main clock /2	15.7	12

Table 14: Main clock configuration and frame rate

In LVDS mode, in order to reliably de-serialize the incoming data, the receiver side should sample the data at least with 750MHz to properly detect the phase of the transitions, and in order to increase the robustness of the de-serialization under the presence of significant jitter, which has to be expected from the on-chip oscillator, the data is EXOR with the data clock.

- **Data Word Encoding**

There are three different words during data transmission:

→ **Data word**: transmitted during Readout phase, after each start line word. It is a 12bits word EXOR gated with the main clock.

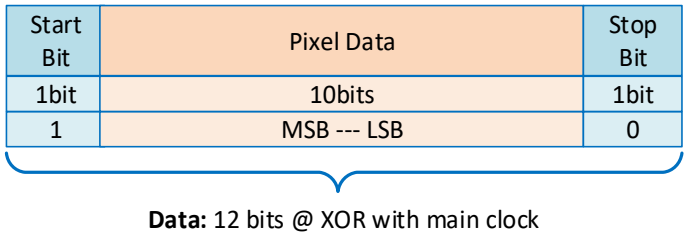


Figure 14: Data word in LVDS transmission mode.

An example of this is:

- 10bits data word: 0110001101
- Including start and stop bits: **1**01100011010
- 12bits word EXOR with the data clock:

  01 01 01 01 01 01 01 01 01 01 01 01 - data clock (main clock)

  11 00 11 11 00 00 00 11 11 00 11 00 - 12bit data @ data clock frequency

  10 01 10 10 01 01 01 10 10 01 10 01 - data word result

→ **Training pattern word**: the training pattern is transmitted during Sync phase, Delay phase, and also during Readout phase as start line identification. It is a 12 bits word with all 0's EXOR gated with the main clock.

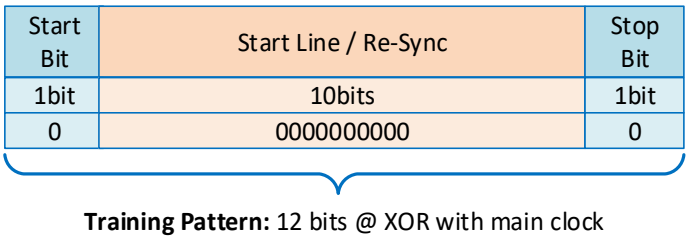


Figure 15: Training Pattern word in LVDS transmission mode.

An example of this is:

- 10bits data word: 0000000000
- Including start and stop bits: **0**00000000000
- 12bits word EXOR with the data clock:

  01 01 01 01 01 01 01 01 01 01 01 01 - data clock (main clock)

  00 00 00 00 00 00 00 00 00 00 00 00 - 12 bit at 0's @ data clock frequency

  01 01 01 01 01 01 01 01 01 01 01 01 - training pattern word result

→ **End of Frame word**: the end of frame word is similar to the training pattern, it is a 12 bits word with all 0's, but in this particular case it is not EXOR with main clock. It is transmitted in the end of the Readout phase.

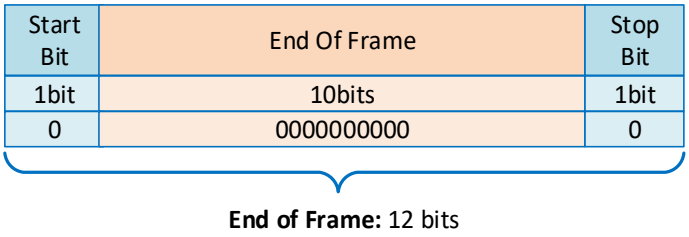


Figure 16: End of Frame word in LVDS transmission mode.

Note that the *start line* identification consists of sending the training pattern 8 times. This results in the following word repeated 8 times:

01 01 01 01 01 01 01 01 01 01 01 01

After the 8PP transmitting the *start line* identification starts the *data* transmission from a particular row. Note that is possible to identify a new row easily by detecting two *ones* after the

eight start lines words. The *ones* appearance results from the last bit of the start line and the first bit of the image data (start bit XOR with data clock) as is shown below:

01 01 01 01 01 01 01 01 01 01 01 01 **1** 10 01 10 10 01 01 01 10 10 01 10 01

The *End of Frame* identification is sent after the last row and before the Serial phase, it is the end of frame word repeated 7 times. The end of frame word is:

00 00 00 00 00 00 00 00 00 00 00 00

The *Re-sync* identification is sent after the Serial phase (SPI communication) in order to restart the sensor synchronism. It will send the training pattern word during 1017PP. Same word is transmitted on Delay phase, during the programmed time.

The principle of the LVDS interface is shown below, Figure 14. To reduce noise coupling to the analogue electronics the LVDS output current is configured between 600uA to 2mA (by serial interface), which will guarantee a save detection and de-serialization based on very low voltage swing LVDS receiver.

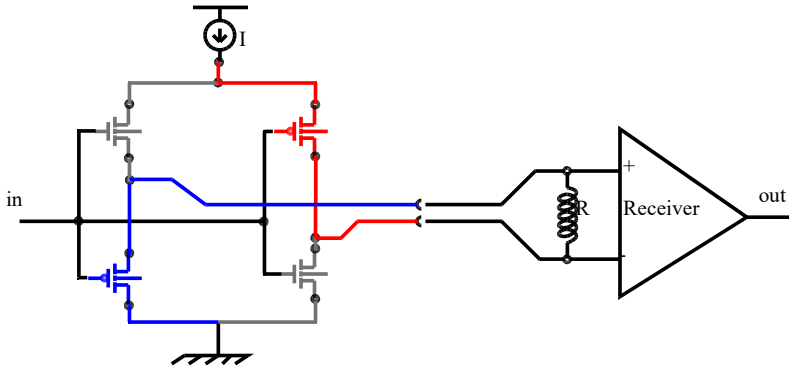


Figure 17: Principle of the LVDS transmitter with current steering scheme.

10.6.3 Data Interface SEIM transmission mode

In SEIM mode the data is transmitted in Single Ended. Data is generated as 10bit representation. Each pixel data is transmitted in a pixel clock, what means a data bit rate at 12 times the pixel frequency. Then the 12bits pixel data word is done adding a start and stop bit to the 10bits.

In SEIM the DATA- line is always configured as an input and receives the bit clock. The pixel clock is internally generated by means of diving this clock by 12. The serial transmission is directly clocked by the provided clock signal, and a new bit is transmitted on each rising edge of the received clock. As the on-chip ADC will still run on the on-chip oscillator, it is the user responsibility to assure the provided clock does not exceed 90% of the nominal clock frequency as a function of the clock division bits given by the table in Table 14: Main clock configuration and frame rate. Lower clock frequencies are possible. While

functionally it may be possible to hold the provided clock, artefacts may occur if the clock frequency is not fixed during operation.

- **Data Word Encoding SEIM**

There are three different words during data transmission:

→ **Data word**: it is a 12 bits word transmitted during Readout mode, after each start of row identification.

Start Bit	Pixel Data	Stop Bit
1bit	10bits	1bit
1	MSB --- LSB	0

Data: 12 bits

Figure 18: Data word in SEIM transmission mode.

An example of this is:

- 10bits data word: 0110001101
- Including start and stop bits: **1**01100011010
- 12bits word:

  10 10 10 10 10 10 10 10 10 10 10 10 - data clock (main clock)

  11 00 11 11 00 00 00 11 11 00 11 00 - data word

→ **Training pattern word**: the training pattern is transmitted during Sync phase, Delay phase, and also during Readout phase as start line identification. It is a 12 bits word.

Start Bit	Start Line / Re-Sync	Stop Bit
1bit	10bits	1bit
0	1010101010	1

Training Pattern: 12 bits

Figure 19: Training Pattern word in SEIM transmission mode.

An example of this is:

- 10bits data word: 1010101010

- Including start and stop bits: **0**10101010101**1**
- 12bits word:

  10 10 10 10 10 10 10 10 10 10 10 10 - data clock (main clock)

  00 11 00 11 00 11 00 11 00 11 00 11 - training pattern word

→ **End of Frame word**: the end of frame word is similar to the training pattern, it is a 12 bits word with all 0's. It is transmitted in the end of the Readout phase.

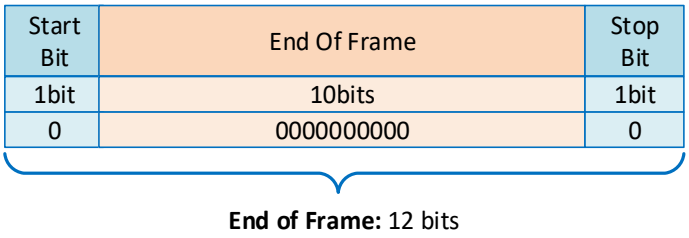


Figure 20: End of Frame word in SEIM transmission mode.

Note that the *start line* identification consists of sending the training pattern 8 times. This results in the following word repeated 8 times:

00 11 00 11 00 11 00 11 00 11 00 11

After the 8PP transmitting the *start line* identification starts the *data* transmission from a particular row. Note that is possible to identify a new row easily by detecting two *ones* after the eight start lines words, as is shown below:

00 11 00 11 00 11 00 11 00 11 00 1111 00 11 11 00 00 00 11 11 00 11 00

The *End of Frame* identification is sent after the last row and before the Serial phase, it is the end of frame word repeated 7 times. The end of frame word is:

00 00 00 00 00 00 00 00 00 00 00 00

The *Re-sync* identification is sent after the Serial phase (SPI communication) in order to restart the sensor synchronism. It will send the training pattern word during 657PP. Same word is transmitted on Delay phase, during the programmed time.

10.7 Timing Characteristics

The timing characteristics for the Osiris M sensor were determined according to the default configuration:

- ✓ ROWS_DELAY_REG[4:0]= '00000', It is 2rows in delay
- ✓ MCLK_MODE_REG[1:0]='01' and HIGH_SPEED_REG[0]='0'. It is 24.7MHz (19FPS)

Each working mode is defined assuming the variables below:

- Sync Mode
  - T_Re-synchronism
- Delay Mode
  - T_Delay
- Readout Mode
  - T_Data
  - T_End_Frame
- Interface Mode
  - T_Serial_Interface

Parameter	Number of Pixel Period	Comment
Pixel Period	1	Pixel Period is defined by 12 main clocks
Main Clock Period	1/12	Transmitted data bit rate
1 Frame	106928	Time for 1 frame
Row Period	328	Time for 1 to 320 rows
T_Re-synchronism	657	Time used for re-synchronism
T_Delay	656	Minimum programmed time for delay (default)
T_Data	104960	Time used for image data
T_End_Frame	7	Time used for End Of Frame identification
T_Serial_Interface	648	Time used for serial communication

Table 15: Readout timings characteristics

11 Register description

There are two register responsible for the programming of the sensor. It is used to set/adjust sensor operation. Note that the registers writing procedure was already explained on a previous section.

11.1 Register 0

Address: 0X000

Default Value: 0x8095

Access: Write Only

Size: 16 bit

Bit	Default Value	Description
15:8	1000000'b	**Rows in Reset** – define the number of rows in reset (ROWS_IN_RST_REG[7:0]) $rows_{\text{in\_rst}} = 2 * \text{ROWS\_IN\_RST\_REG}[7:0] + 2$
7:6	10'b	**VRST Pixel Voltage** – define the reset voltage for pixel (VRST_PIX_REG[1:0]) See Table 15.
5:4	01'b	**Ramp Gain** – define the analogue ramp gain (RAMP_GAIN_REG[1:0]). See Table 16.
3:2	01'b	**Ramp Offset** – define the ramp offset value (OFFSET_RAMP_REG[1:0]). See Table 17.
1:0	01'b	**LVDS Current** – set the LVDS output current (LVDS_CURR_REG[1:0]). See Table 18.

Table 16: Register 0

- **VRST Pixel Voltage**

Bit[1]	Bit[0]	VRST Pixel Voltage [V]
0	0	2.2
0	1	2.4
1	**0**	**2.6 (recommended)**
1	1	3.3

Table 17: Register 0 – VRST Pixel Voltage

- **Ramp Gain**

MCLK [MHz]	Bit[1]	Bit[0]	Ramp Gain (1/Ramp Swing)
12	0	0	0.79
	0	1	0.99
	1	0	1.32
	1	1	1.97
25	0	0	0.80
	0	**1**	**1.00**
	1	0	1.33
	1	1	2.00
49	0	0	0.83
	0	1	1.03
	1	0	1.38
	1	1	2.07

Table 18: Register 0 – Ramp Gain When High Speed is off

MCLK [MHz]	Bit[1]	Bit[0]	Ramp Gain (1/Ramp Swing)
16	0	0	0.79
	0	1	0.99
	1	0	1.32
	1	1	1.97
31	0	0	0.81
	0	**1**	**1.01**
	1	0	1.35
	1	1	2.03
63	0	0	0.83
	0	1	1.04
	1	0	1.39
	1	1	2.10

Table 19: Register 0 – Ramp Gain When High Speed is on

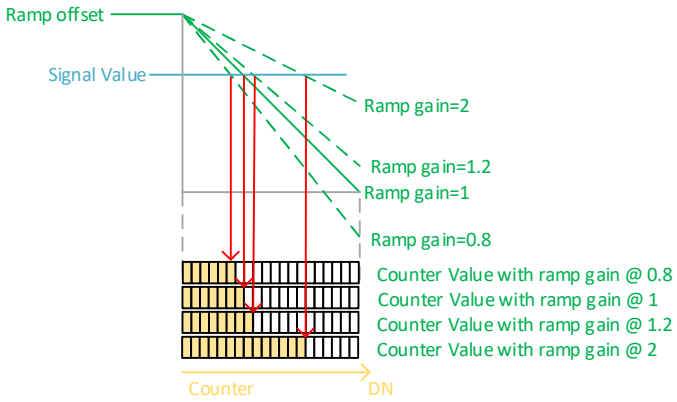


Figure 21 : Register 0 - ADC ramp gain configuration

- **Ramp Offset**

Bit[1]	Bit[0]	Ramp Offset Voltage [V]
0	0	1.9
0	**1**	**2**
1	0	2.1
1	1	2.2

Table 20: Register 0 – Ramp Offset

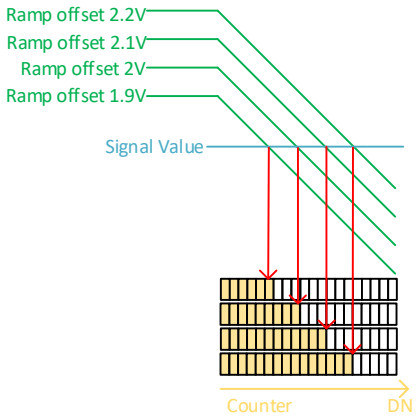


Figure 22: Register 0 - ADC ramp offset configuration

- **LVDS Current**

Bit[1]	Bit[0]	LVDS Current [uA]
0	0	600
0	**1**	**1200**
1	0	1800
1	1	2000

Table 21: Register 0 – LVDS Current

11.2 Register 1

Address: 0X001

Default Value: 0x0064

Access: Write Only

Size: 16 bit

Bit	Default Value	Description
15:11	00000'b	**Delay Programmable** – define the number of rows period in delay mode (ROWS_DELAY_REG[4:0]) $rows_{delay} = 16 * \text{ROWS\_DELAY\_REG}[4:0] + 2$
10:10	0'b	**Bias Current Increase** – when set to '1' it will increase the different bias currents to approximately. the double of nominal values
9:9	1'b	**CDS Gain** – when set to '1' the CDS presents a gain of 2, otherwise the CDS gain is 1.3 (recommended is 1.3)
8:8	1'b	**Output Mode** – defines output as LVDS MODE('1') or SEIM('0')
7:6	01'b	**Main Clock Configuration** – define the main clock frequency (MCLK_MODE_REG[1:0]) See Table 20.
5:4	01'b	**VREF for Signal** – define the reference voltage for CDS (Correlated Double Sampling) (VREF_REG[1:0]) See Table 21.
3:2	10'b	**CVC Current** – define the CVC current (CVC_CURRENT_REG[1:0]) See Table 22.
1	1'b	**Idle Mode –** define if the sensor is working in an idle mode (lower power consumption) or not ((IDLE_MODE_REG[0])) 0 – Disabled Idle Mode 1 – Enabled Idle Mode

0	0'b	**High Speed Clock** – when it is enabled ('1') the clock works in a high speed mode (HIGH_SPEED_REG[0])

Table 22: Register 1

- **Main Clock Configuration & High Speed Clock**

MCLK_MODE_REG[1:0]		HIGH_SPEED_REG[0]	Description	MCLK [MHz]	Frame Rate [FPS]
Bit[1]	Bit[0]				
0	0	**0**	Main Clock times 2	49.1	38
0	**1**		**Default value**	**24.7**	**19**
1	0		Main Clock dividing by 2	12.3	9
1	1		Main Clock dividing by 2	12.3	9
0	0	1	Main Clock in high speed mode times 2	62.6	49
0	1		Main Clock for high speed mode	31.1	24
1	0		Main Clock in high speed mode dividing by 2	15.7	12
1	1		Main Clock in high speed mode dividing by 2	15.7	12

Table 23: Register 1 – Main Clock

- **VREF for signal**

Bit[1]	Bit[0]	VREF CDS [V]
0	0	1.9
0	**1**	**2**
1	0	2.1 (recommended)
1	1	2.2

Table 24: Register 1 – VREF CDS

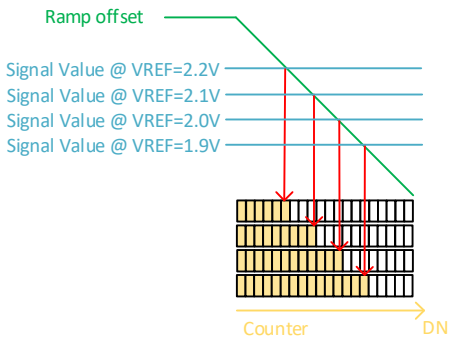


Figure 23: Register 1 - VREF CDS configuration

- **CVC Current**

Bit[1]	Bit[0]	MCLK [MHz]	CVC Current [uA]
0	0	12	0.36
0	1		0.79
1	0		0.98
1	1		1.44
0	0	**25**	0.69
0	**1**		**1.58**
1	0		1.98
1	1		2.93
0	0	49	1.54
0	1		3.18
1	0		4.06
1	1		6.07
0	0	16 High speed	0.46
0	1		1.03
1	0		1.29
1	1		1.88
0	0	31 High speed	0.90
0	1		2.05
1	0		2.59
1	1		3.85
0	0	63 High speed	1.75
0	1		4.14
1	0		5.30
1	1		7.95

Table 25: Register 1 – CVC Current

- **Idle Mode**

Bit[0]	Comment	Power Consumption
0	Idle mode off	12mW (LVDS output mode)
		9.7mW MCLK 25MHz SEIM
1	Idle mode on	3.2mW

Table 26: Register 1 – Idle Mode On/OFF – power consumption

- **CDS gain**

Bit[0]	Comment
0	CDS gain is 1.3
1	CDS gain is 2

Table 27: Register 1 - CDS gain

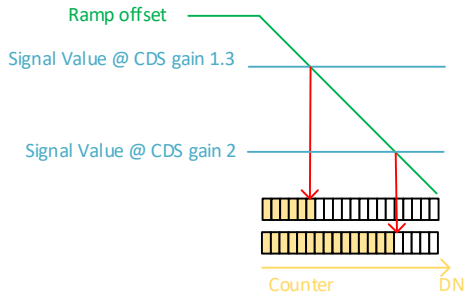
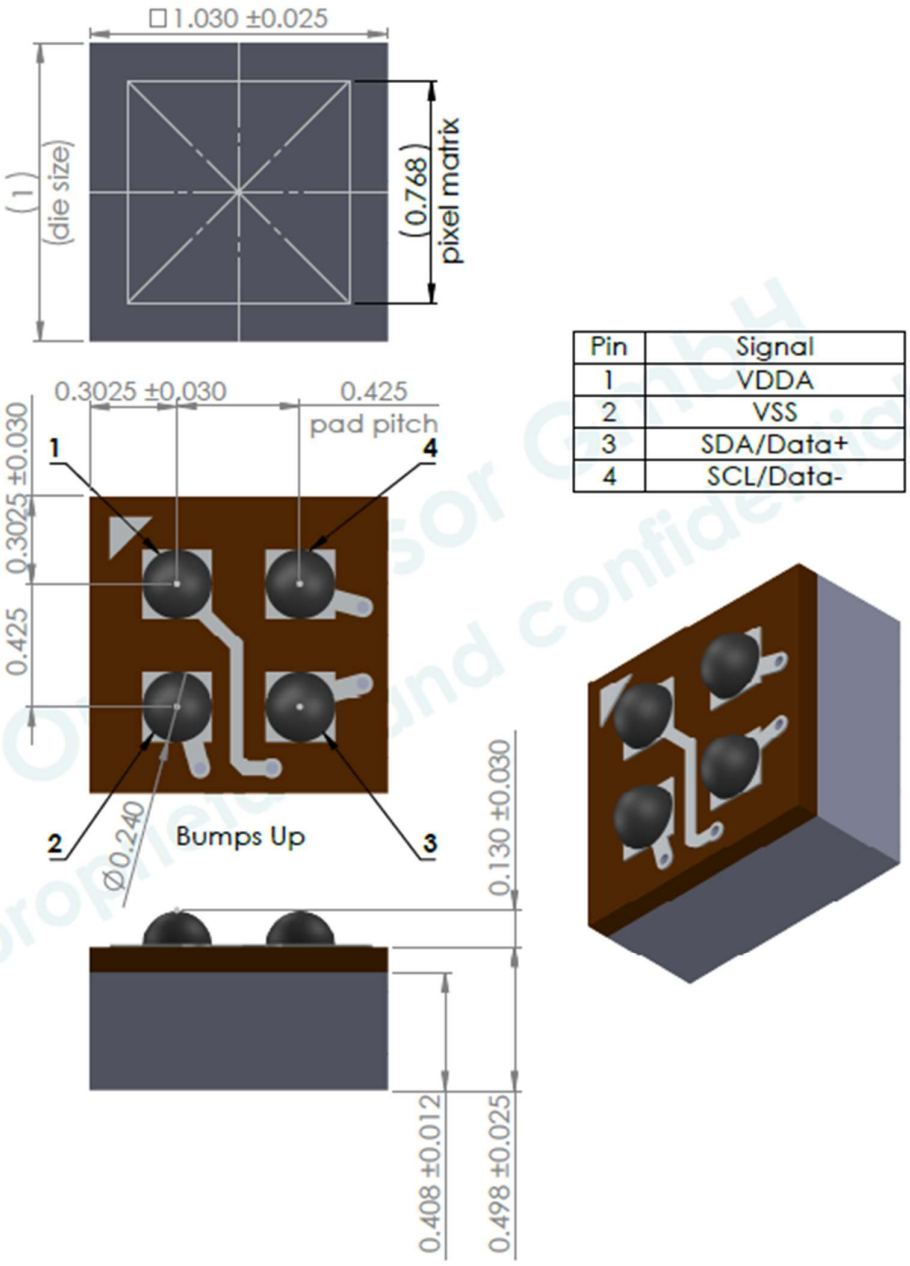


Figure 24: Register 1 - CDS gain configuration

12 Mechanical drawings and pinout table



Pin	Signal
1	VDDA
2	VSS
3	SDA/Data+
4	SCL/Data-

Figure 25: Chip Osiris M mechanical drawings

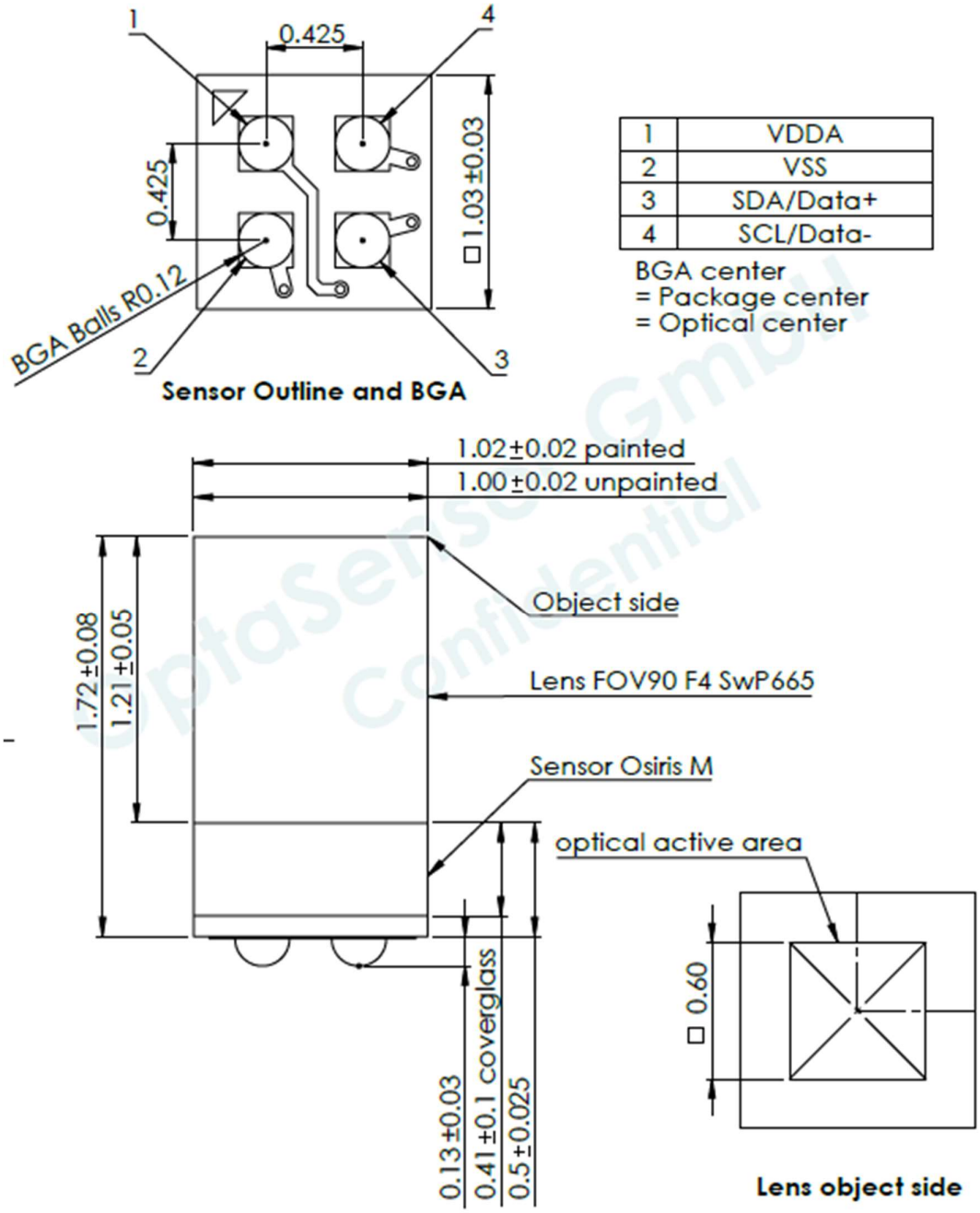


Figure 26: Camera Osiris M FOV90 F4.0 with infrared cut

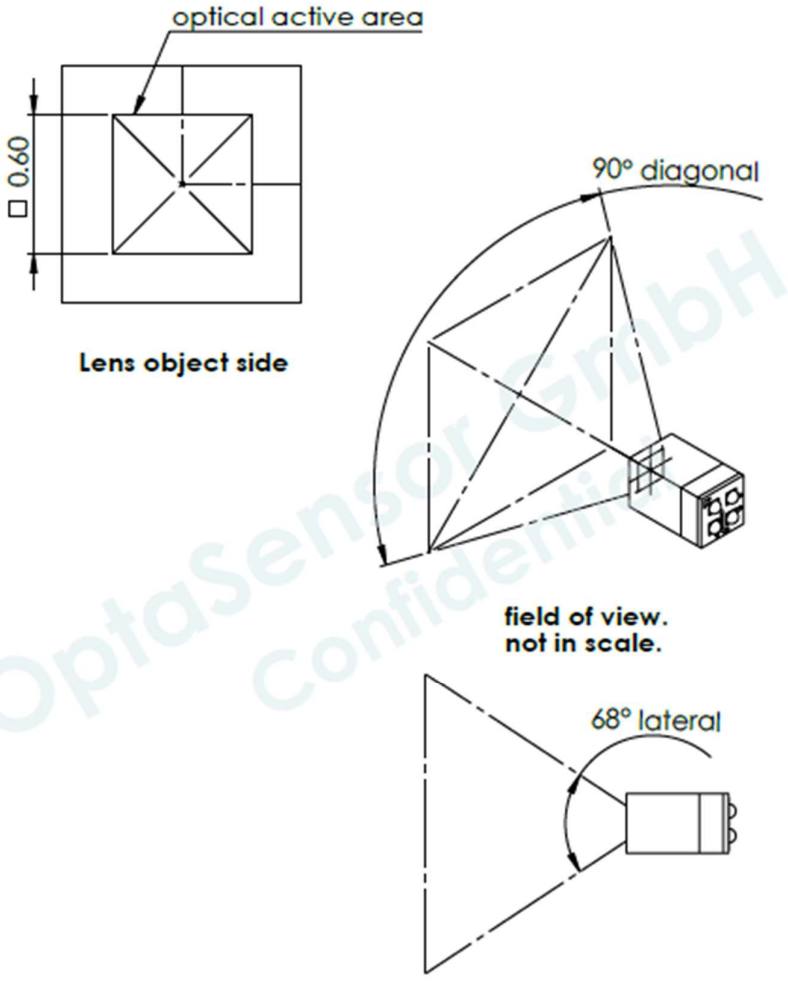


Figure 27: Camera Osiris M FOV90 F4.0 with infrared cut (FOV cone)

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